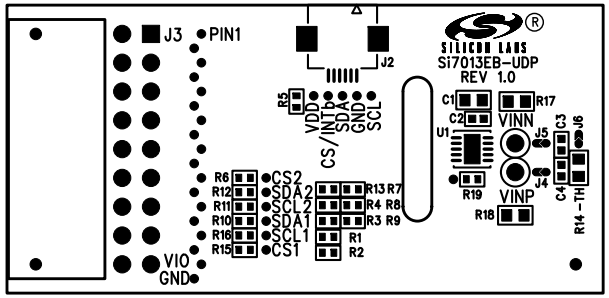
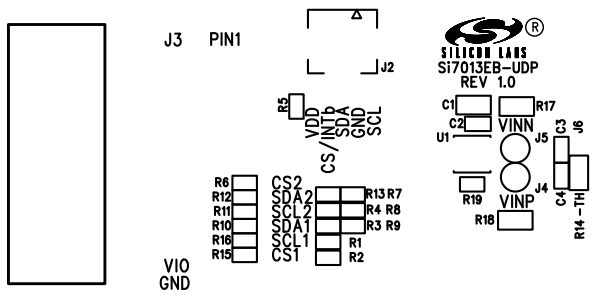

J3
PIN1
J2
SILICON LABS
Si7013EB-UDP
REV 1.0
R5
VDD
CS/INT
SDA
GND
SCL
C1
R17
C2
VINN
U1
J5
C3
J6
R6
CS2
R12
SDA2
R13
R7
R11
SCL2
R4
R8
R10
SDA1
R3
R9
R16
SCL1
R1
R15
CS1
R2
R19
J4
C4
R14 - TH
R18
VINP
VIO
GND


J3
PIN1
J2
SILICON LABS
Si7013EB-UDP
REV 1.0
R5
VDD
CS/INTb
SDA
GND
SCL
C1
R17
C2
U1
VINN
J5
C3
J6
R6
CS2
R12
SDA2
R13
R7
R11
SCL2
R4
R8
R10
SDA1
R3
R9
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R1
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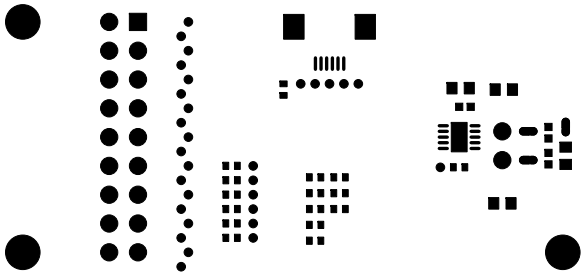
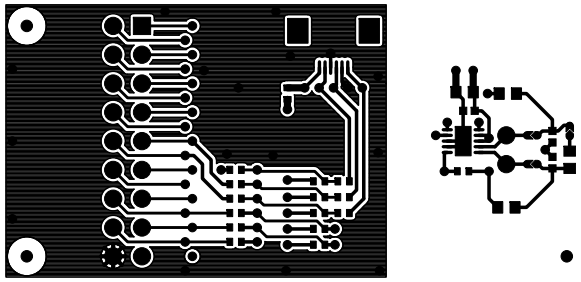
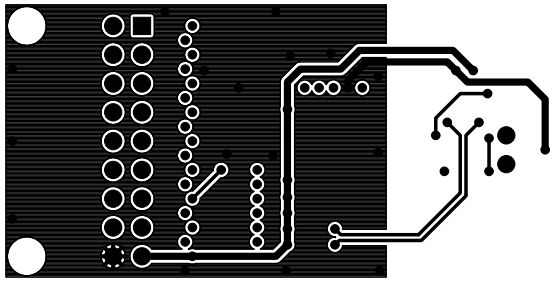
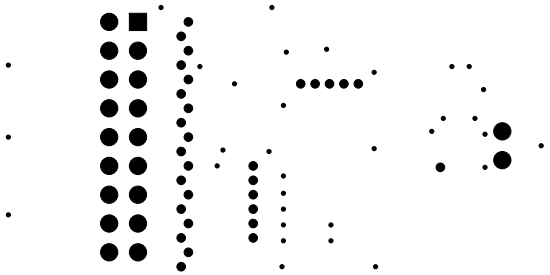
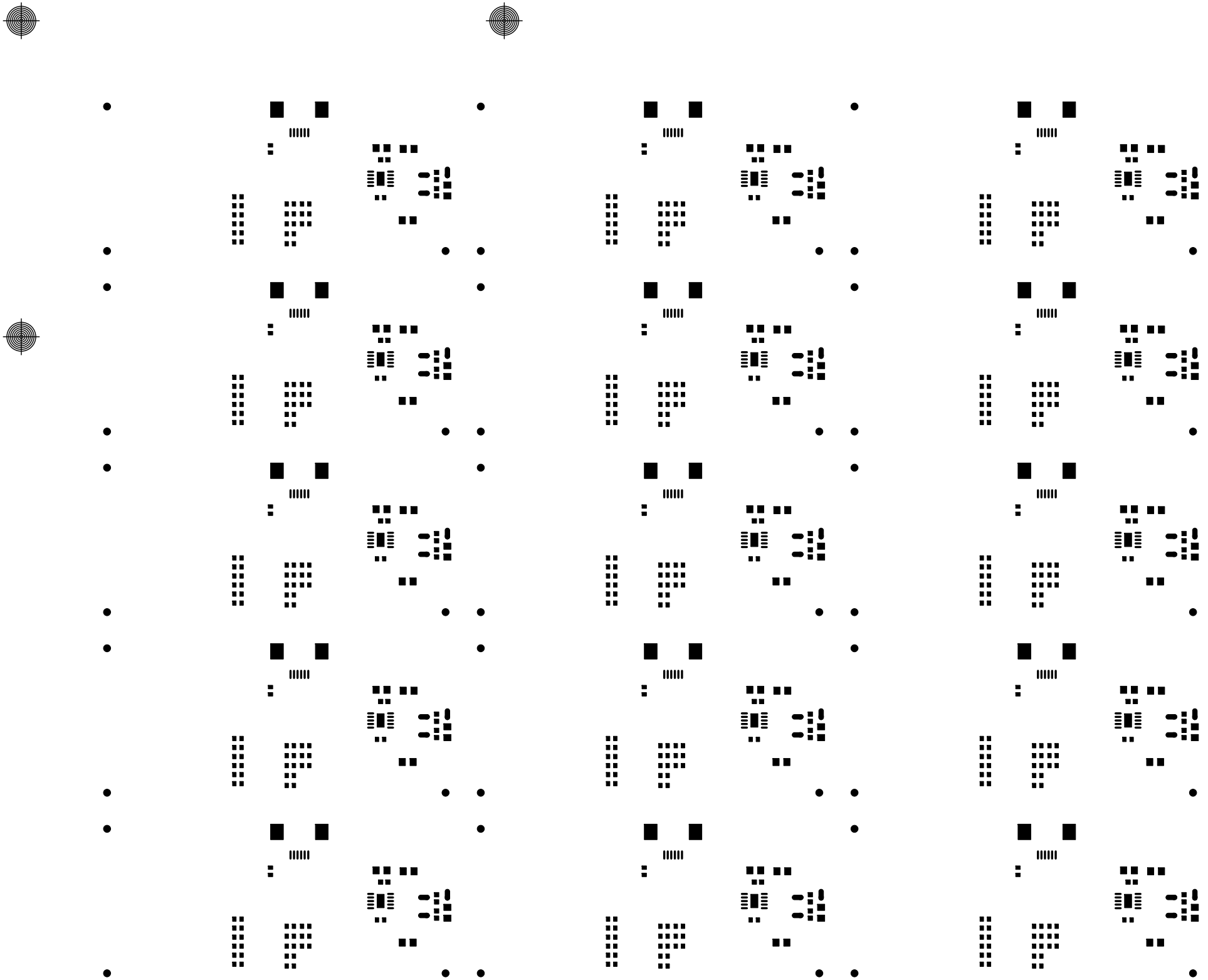
CS1
R2
R19
VINP
J4
C4
R18
R14 - TH
VIO
GND

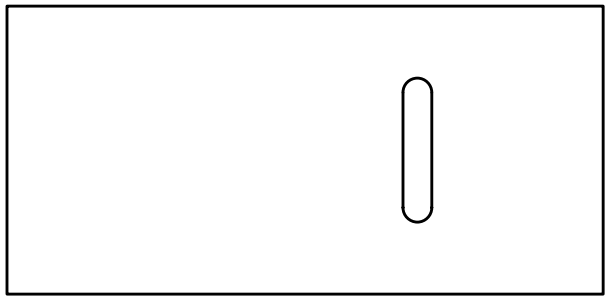


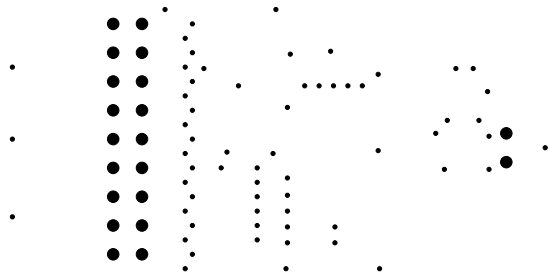






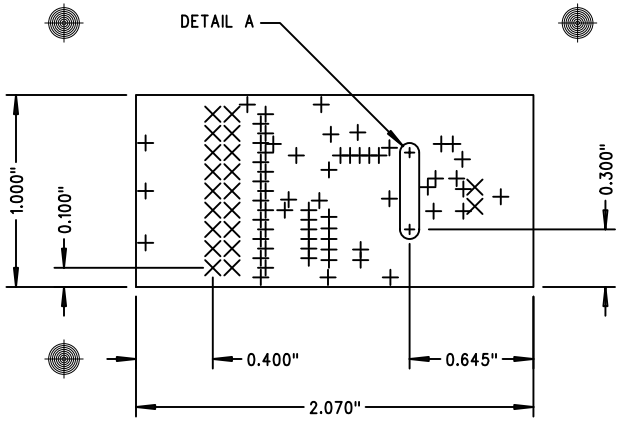






NOTES : UNLESS OTHERWISE SPECIFIED

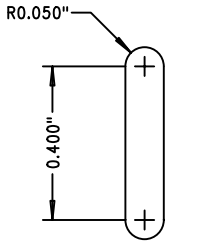
1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. MATERIAL SHALL BE COPPER CLAD FR-4, NEMA GRADE PER IPC-4101/26, COLOR NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, RED SOLDER MASK OVER OXIDIZED COPPER, HASL BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT



LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	7013EB-UDP_PSS.PHO
PRIMARY SOLDERMASK	7013EB-UDP_PSM.PHO
PRIMARY SIDE	7013EB-UDP_PRI.PHO
SECONDARY SIDE	7013EB-UDP_SEC.PHO
SECONDARY SOLDERMASK	7013EB-UDP_SSM.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.015	63	+	P	1	+0/-0.015
0.040	20	×	P	2	+/-0.003



DETAIL A

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER MIL-D-1000

TOLERANCES

HOLE TOLERANCES PER 78027

DECIMALS	ANGLES	SURFACES
.XX +/- .XXX +/-	+/-	MICROINCHES

PART TO BE FREE OF BURRS

BREAK EDGES	BEND RADIUS	BEND RELIEF
MAX	MAX	MAX

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC..

DESIGN	JG	22APR2013
LAYOUT	CT	22APR2013

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W Cesar Chavez
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

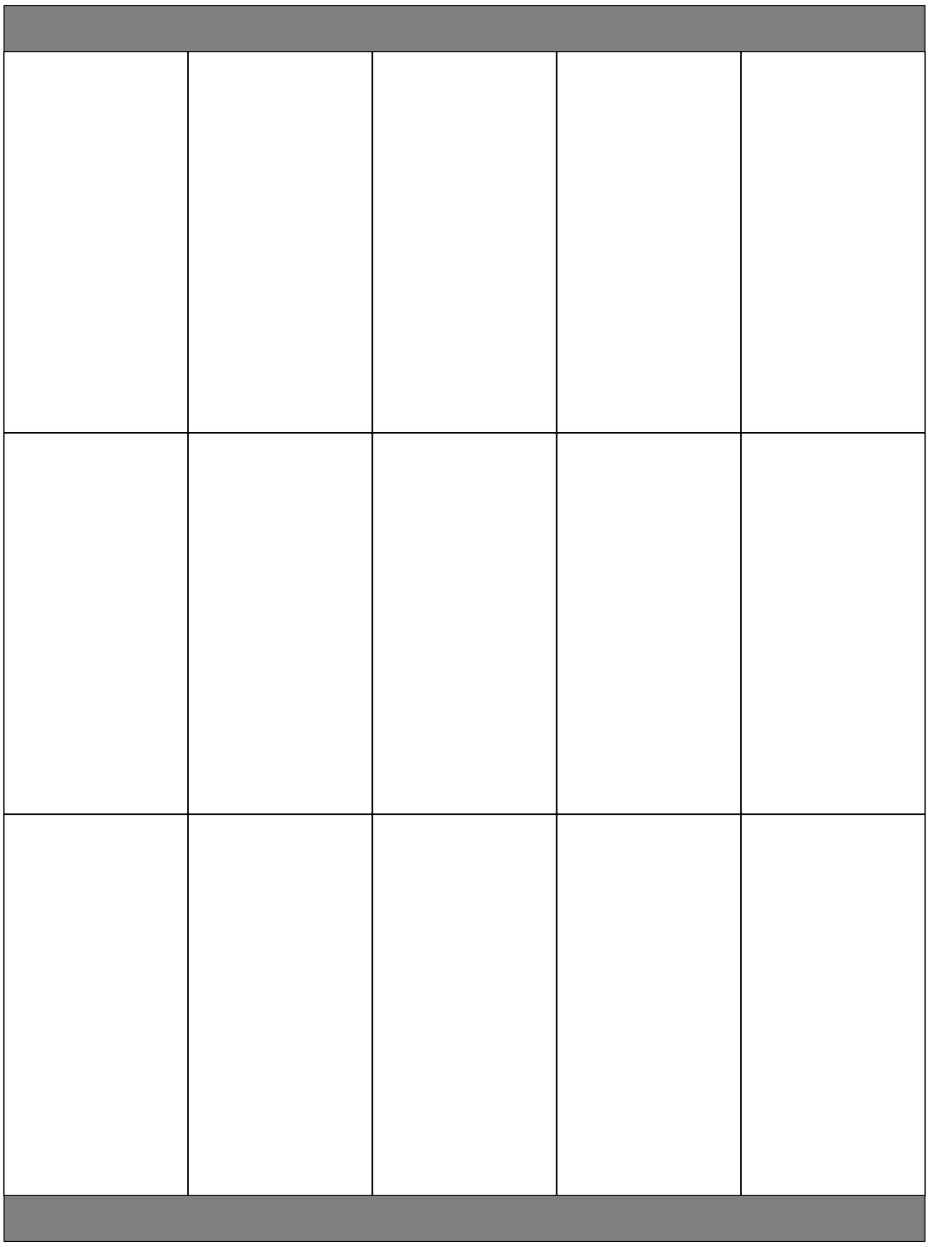
NAME: Si7013EB-UDP

REV : 1.0

SIZE A

PART NUMBER:

SCALE 1:1 | FABRICATION DRAWING | SHEET 1 OF 1



Si7013EB-UDP REV 1.0

Size:
Array: 5.0 x 6.71
Part: 1.0 x 2.07

Parts On Array:
15 Parts

Matrix:
5 x 3

Spacing:
0.0 x 0.0

Array Borders:
Left: 0.0 Right: 0.0
Top: 0.25 Bottom: 0.25

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduials to each side of array located 0.25" from tooling holes.