AN203: 8-bit MCU Printed Circuit Board Design Notes

The tips and techniques included in this application note will help to ensure successful printed circuit board (PCB) design.

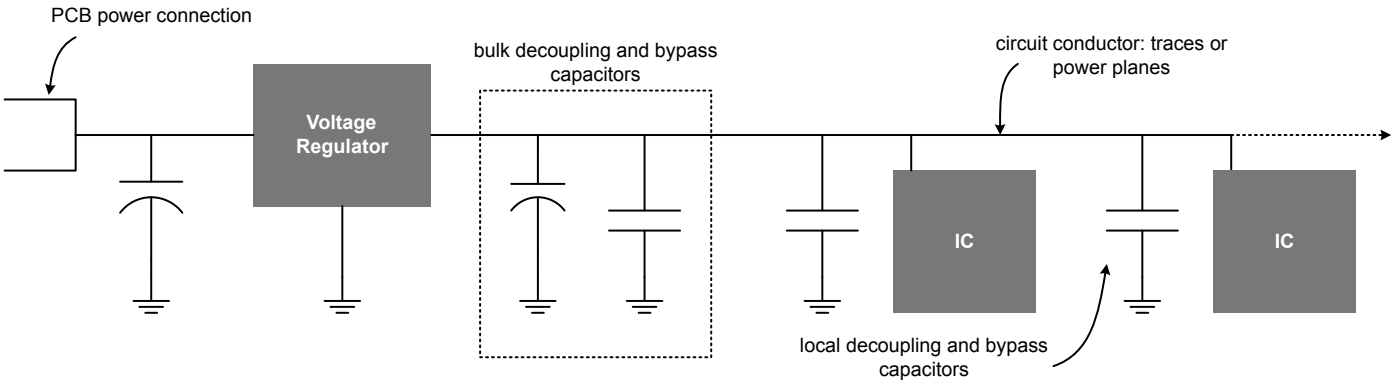
Problems in design can result in noisy and distorted analog measurements, error-prone digital communications, latch-up problems with port pins, excessive electromagnetic interference (EMI), and other undesirable system behavior.

The methods presented in this application note should be taken as suggestions which provide a good starting point in the design and layout of a PCB. It should be noted that one design rule does not necessarily fit all designs. It is highly recommended that prototype PCBs be manufactured to test designs. For further information on any of the topics discussed in this application note, please read the works cited in 11. References.

The information in this application note applies to all 8-bit MCUs (EFM8 and C8051).

KEY POINTS

- Power and ground circuit design tips.
- Analog and digital signal design recommendations with special tips for traces that require particular attention, such as clock, voltage reference, and the reset signal traces.
- Special requirements for designing systems in electrically noisy environments.
- Techniques for optimal design using multilayer boards.
- A design checklist.



1. Power and Ground

All embedded system designs have a power supply and ground circuit loop that is shared by components on the PCB. The operation of one component can affect the operation of other components that share the same power supply and ground circuit [1].

1.1 Power Supply Circuit

The goal of an embedded system's power supply is to maintain a voltage within a specified range while supplying sufficient current. While an ideal power supply would maintain the same voltage for any possible current draw, real world systems exhibit the following non-ideal behaviors:

- A change in current and its associated noise caused by one device affects other devices attached to the same power supply net.
- A change in current draw affects the voltage of the power net.
- Improper use of voltage regulator devices can result in supply voltage instability.

The typical power supply circuit consists of the following:

- A PCB power supply connection with decoupling and filter components.
- Voltage regulators that maintain voltage within a required range while supplying sufficient current to all components served.
- Voltage supply bulk decoupling and bypass capacitors.
- Power and supply circuit traces or a power supply plane that distributes power to the components.
- Local decoupling and bypass capacitors at each integrated circuit (IC).
- Optional power supply filters placed between different power supply circuits.

Design tips for each of these components can be found in the following subsections. For a detailed discussion on capacitors, see 8. Appendix B—Capacitor Choice and Use.

1.1.1 Voltage Regulator

A voltage regulator takes an input voltage from a source external to the system and outputs a defined voltage that can power components on the circuit board. Two common types of voltage regulators are dc-dc converters and low-dropout regulators. When deciding on a voltage regulator, always review the regulator data sheets to match component specifications with system requirements.

Switched Capacitor DC-DC Converters

The high efficiency of this type of regulator makes it an ideal choice for designs where power conservation is an issue, such as battery-powered applications. However, switching supplies introduce high-frequency noise to the power supply net. This noise can be reduced by filtering and by adding bypass capacitors. On boards using this type of regulator, ADC performance is minimally affected by power supply noise by synchronizing the ADC's sampling rate with the power supply's switch time.

Low-Dropout Regulators

Low-Dropout Regulators (LDOs) are less efficient than dc-dc converters, but they also introduce less noise into the power circuit. Silicon Labs' example boards typically use a low-dropout regulator, which maintains voltage within the microcontroller's specified range while providing a large amount (~500 mA) of current.

1.1.2 Power Supply Bulk Decoupling and Bypassing

Noise can be introduced into the power circuit from the voltage regulator from ICs connected to the net and from electromagnetic noise that couples into the power supply trace loops. Power supply bulk decoupling capacitors help to minimize the effects of noise and provide other benefits to the circuit as well. Figure 1.1 PCB Power Supply Circuit with Decoupling, Bypassing, and Isolation—Series on page 2 shows a typical decoupling circuit design with the analog and digital supplies in series, favoring the analog supply. If the digital supply is not expected to be noisy, then a parallel configuration shown in Figure 1.2 PCB Power Supply Circuit with Decoupling, Bypassing, and Isolation—Parallel on page 3 is also acceptable.

Large bulk capacitors improve performance during lowfrequency fluctuations in supply current draw by providing a temporary source of charge. These capacitors can supply charge to local IC decouple/bypass capacitors.

Many voltage regulators maintain their voltage by using a negative feedback loop topology that can become unstable at certain frequencies. A capacitor placed at the regulator's output can prevent the voltage supply from becoming unstable. Check the regulator's data sheet for recommended capacitor specifications.

Bulk decoupling capacitors should be placed close to the output pin of the voltage regulator. Typically, the power supply decoupling capacitance value should be 10 times that of the total capacitance of the decoupling capacitors local to each IC. Tantalum or electrolytic capacitors are commonly used for bulk decoupling.

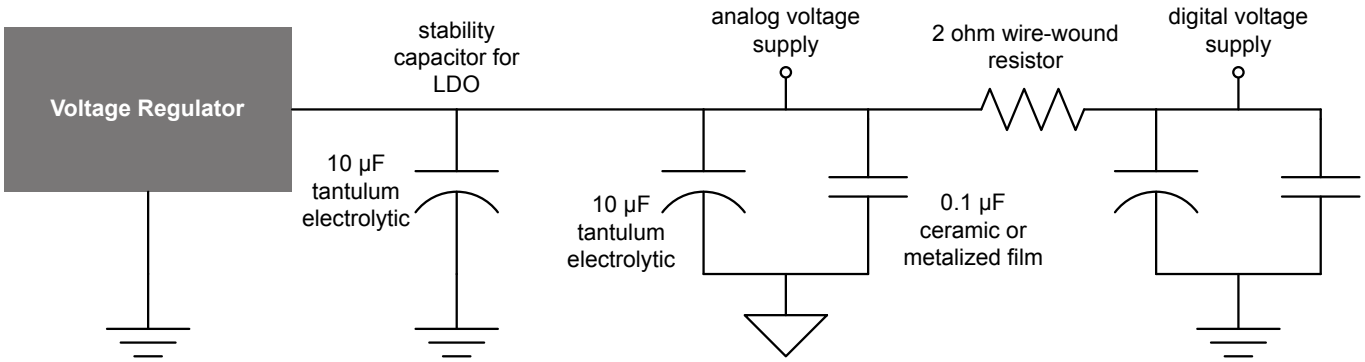


Figure 1.1. PCB Power Supply Circuit with Decoupling, Bypassing, and Isolation—Series

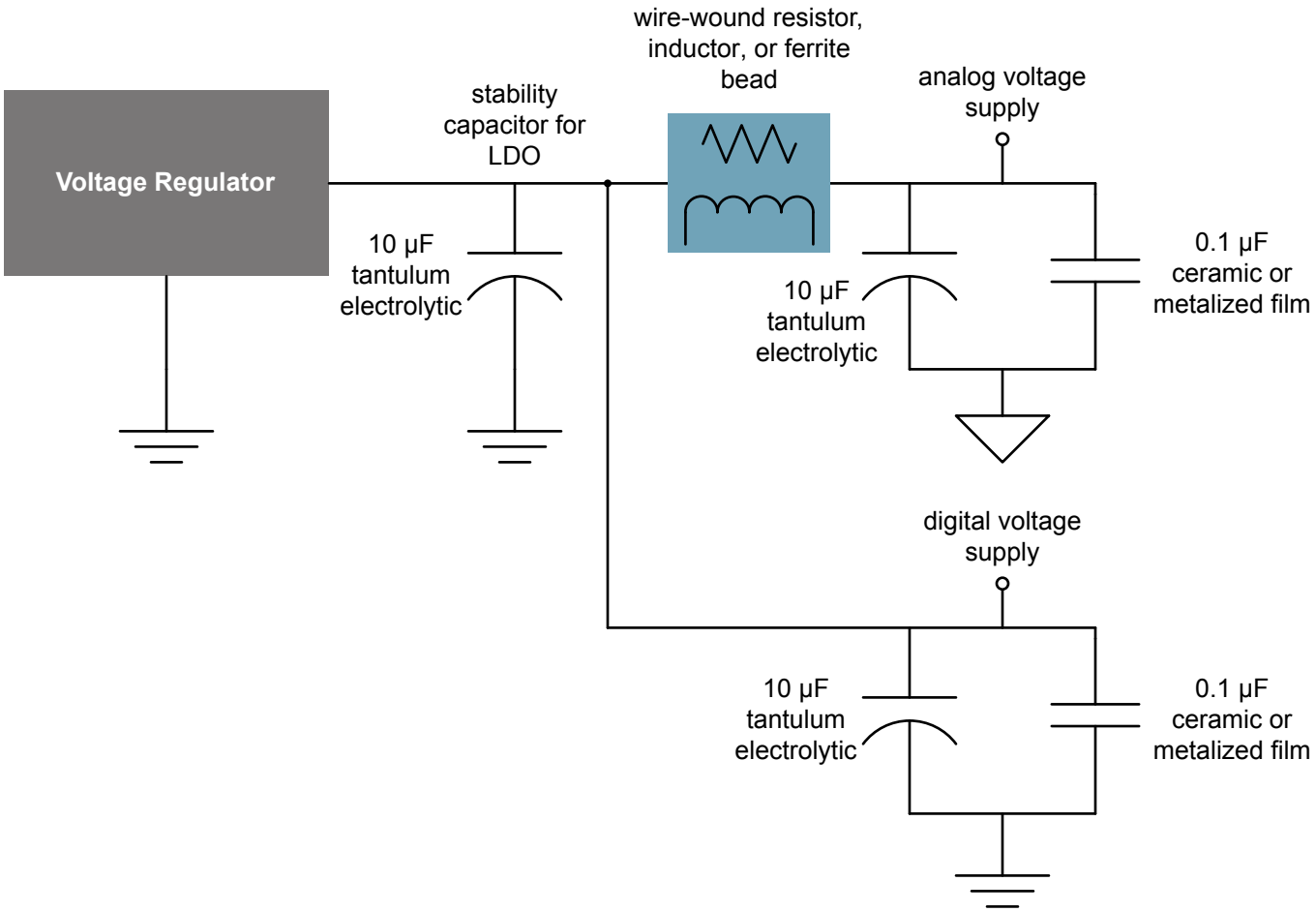


Figure 1.2. PCB Power Supply Circuit with Decoupling, Bypassing, and Isolation—Parallel

To help filter high-frequency digital and EMI noise, a bypass capacitor with a capacitance that is one or two orders of magnitude smaller than the bulk decoupling capacitor should be placed in parallel with the bulk decoupling capacitor. The lower value capacitor shunts high-frequency noise coupled on the power supply traces to ground due to its low impedance in the higher frequency range.

1.1.3 IC Decoupling and Bypassing

As digital logic gates of ICs switch from one state to another, the IC's current draw fluctuates at a frequency determined by the logic state transition rate or rise time. These changes cause the power supply voltage to fluctuate because the traces connecting the net have a characteristic impedance.

The circuit's impedance can be lowered by adding capacitance to the power supply circuit that provides a low-impedance path to ground for high frequencies. See 7. Appendix A—Rise Time-Related Noise for a more detailed explanation.

1.1.4 Power Supply Filtering

Filters can be added to the power supply circuit to provide components with further immunity to high-frequency noise. Figure 1.3 Voltage Supply Filter Examples on page 4 shows two commonly used lowpass filter topologies.

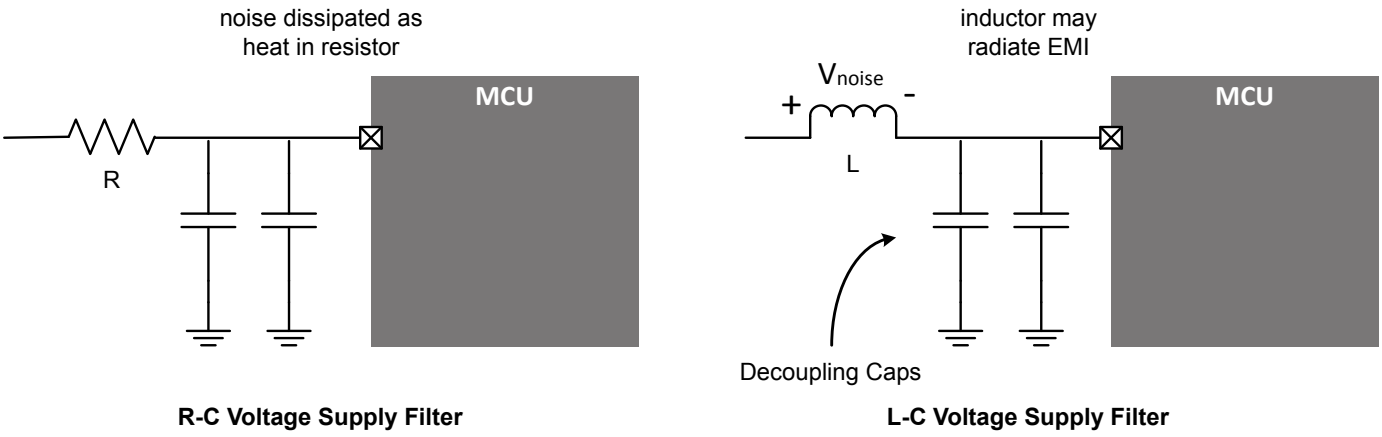


Figure 1.3. Voltage Supply Filter Examples

LC filters force the noise voltage to appear across the inductance rather than across the device or main power supply circuit. A ferrite bead can be used to provide the inductance. Since LC filters are reactive, they can actually increase noise at the filter's resonant frequency, and the noise across the inductor increases the EMI radiated by the circuit [1].

RC filters dissipate the noise by converting it to heat. Therefore, the circuit radiates less EMI compared to LC filters [1]. However, RC filters create a larger dc voltage drop than LC filters in the supplied voltage for a given filtering capability. RC filters are typically less expensive than LC filters.

The loop area from the voltage supply pin to decoupling capacitor to ground should be kept as small as possible by placing the capacitor near the power supply pin and ground pin of the device. For an example layout of decoupling capacitors, see Figure 1.4 Minimize Loop Area between Power and Ground on page 4.

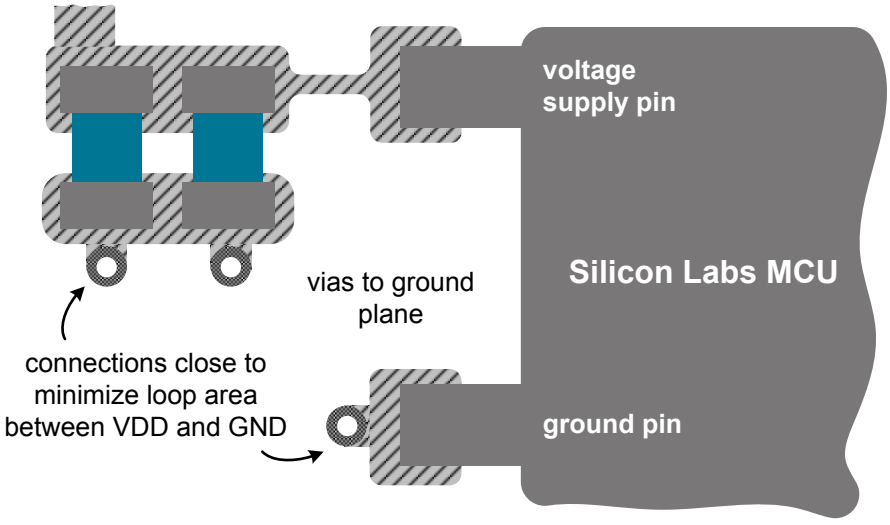


Figure 1.4. Minimize Loop Area between Power and Ground

1.1.5 Filtering Considerations for Mixed-Signal ICs

Mixed-signal embedded systems have both analog and digital voltage supplies that often share a common regulator. Through this shared power net, high-frequency digital noise can couple into the analog circuit and corrupt analog measurements. Filtering or isolating the analog power circuit can eliminate this coupling.

In-series inductance provides the most effective isolation from high-frequency noise. The inductance should be placed between the analog and digital power supply circuits, with the analog circuit closest to the voltage regulator. If, due to cost or lack of availability, it is not practical to use an inductor, a low value (~2 Ω) wirewound resistor can also be used because of the resistor's inherent parasitic inductance. Figure 1.5 Filtering Analog Power Supply on page 5 shows an example of analog power supply filtering.

PCBs should always be designed with a place for bypass capacitor(s), in case they are needed, and removed or tested with different capacitor values should the PCB have a large amount of digital noise coupling into analog circuits.

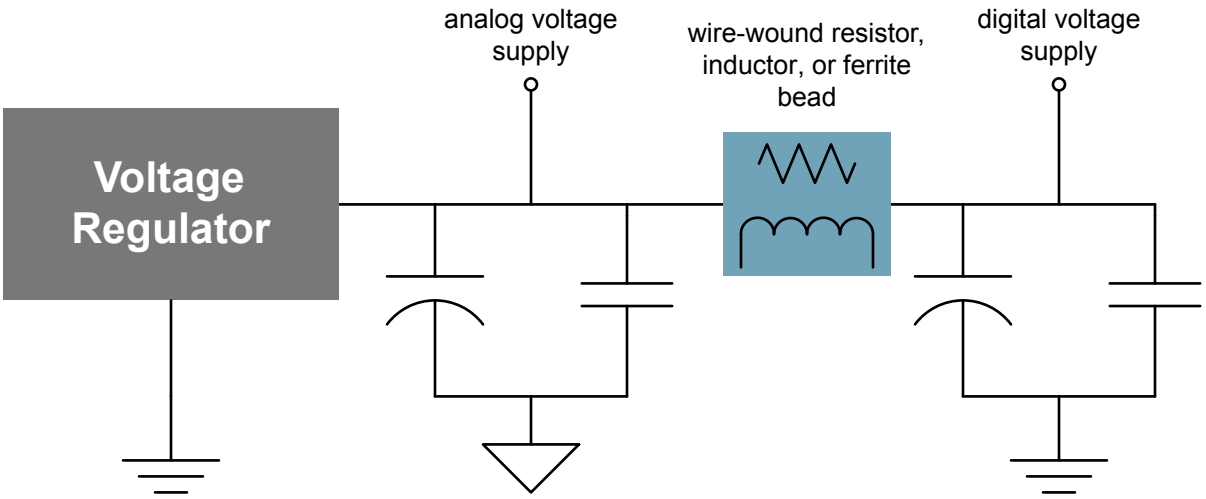


Figure 1.5. Filtering Analog Power Supply

1.2 Ground Circuits

The ground circuit can introduce noise to an embedded system and affect components. An ideal ground circuit is equipotential, meaning that the voltage of the circuit does not change regardless of the current. Real-world ground circuits have a characteristic impedance and experience changes in voltage with changes in current. Careful PCB design can minimize this non-ideal behavior to create a ground circuit that provides a low impedance return path for current.

1.2.1 Designing with a Ground Plane

While some systems connect components to a ground circuit through wires or traces, most designs use a ground plane in which the PCB's components connect their ground pins to a common conductive plane. Design with a ground plane is highly recommended for two reasons:

- The return current noise of one device has less effect on other components.
- Short connections minimize the voltage drops caused by inductance and resistance in the return path.

1.2.2 Ground Plane Fill

A ground plane should cover as much of the board as possible, even in spaces between devices and traces. Islands of copper formed between traces or devices should always be connected to ground and should never be left floating. Spreading the ground plane across the board also aids in noise dissipation and shields traces. If possible, the ground plane should also be placed under the MCU package.

1.2.3 Separate Mixed-Signal Ground Planes

Separating the analog current return path from the noisier digital current return path can improve analog measurements. Ground isolation can also improve performance in boards connected to industrial or noisy systems. Separate ground planes should be connected in only one location, usually near the power supply. Figure 1.6 Using Split Analog and Digital Ground Planes on page 6 shows the use of a split analog and digital ground circuit example.

Note: Splitting the ground planes can improve noise if there are no high-speed digital signals crossing between planes. If these signals do exist, splitting the planes forces the return current though a much longer path, which will result in higher EMI. Instead, a single ground plane is recommended in these cases.

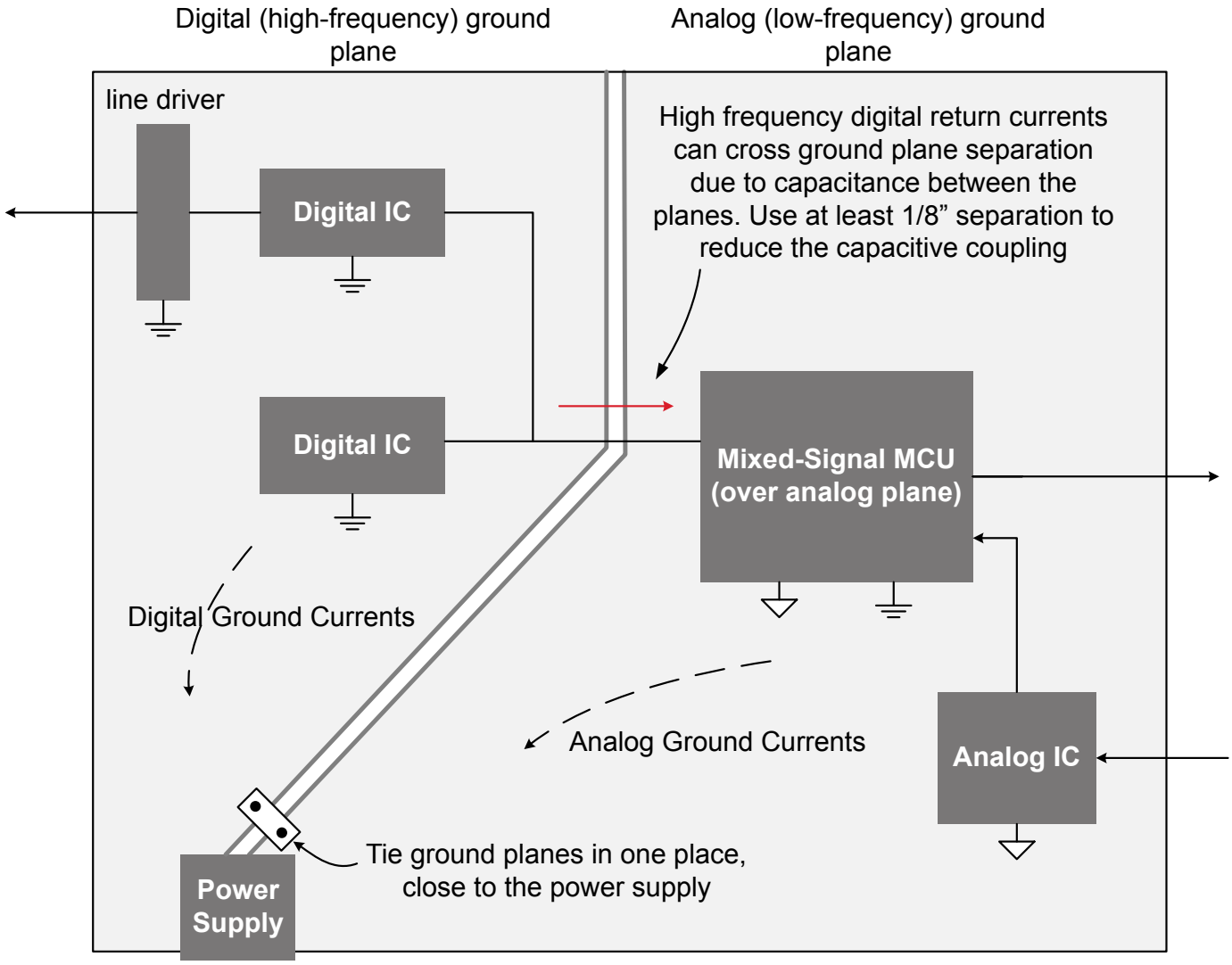


Figure 1.6. Using Split Analog and Digital Ground Planes

If possible, the mixed-signal MCU should be placed entirely in the analog ground plane. The MCU may also reside over both planes, with the divide running under the device.

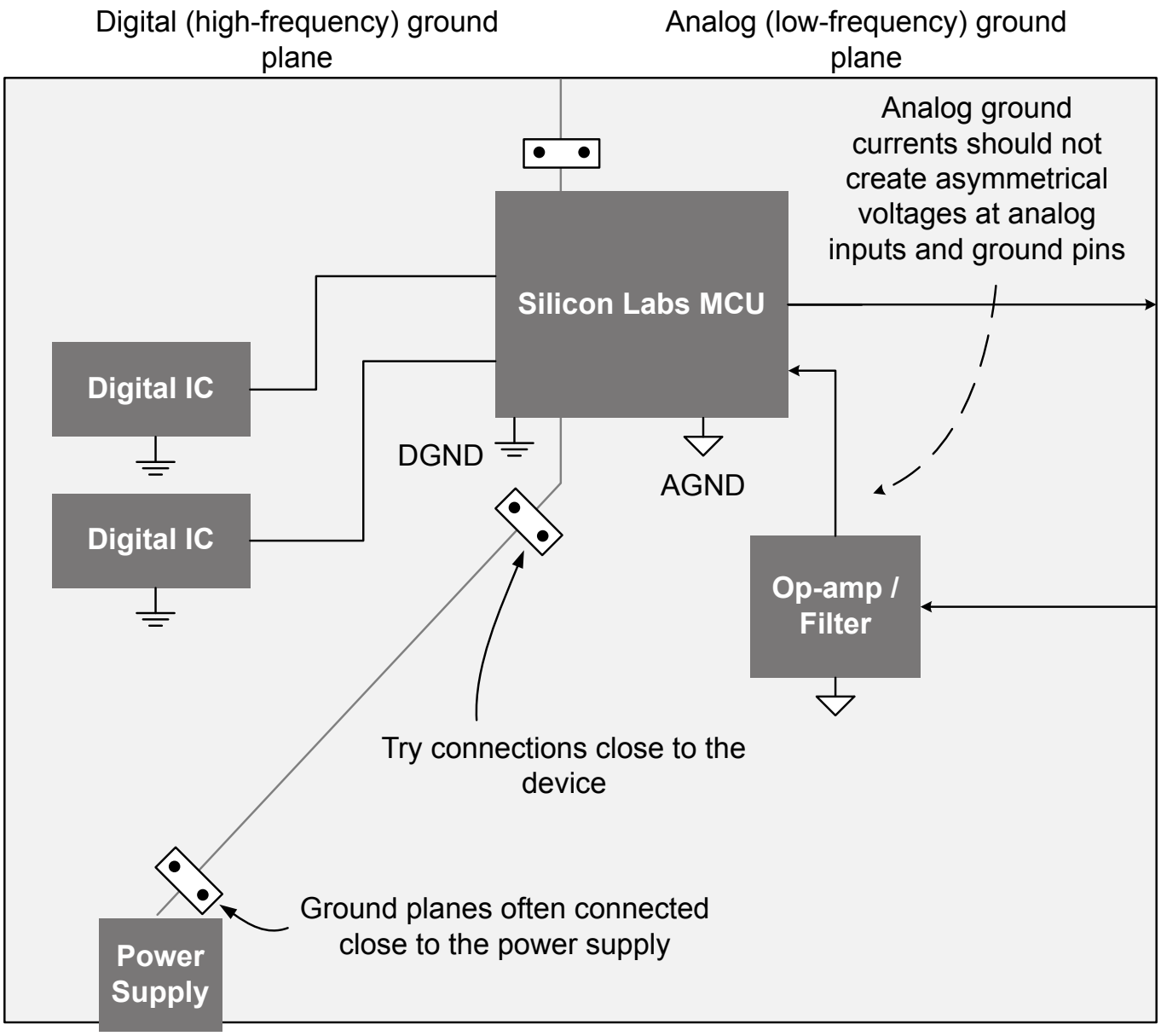


Figure 1.7. Placing the Microcontroller on both Analog and Digital Ground Planes

1.2.4 Shared Mixed-Signal Ground Planes

Not all mixed signal embedded systems require separate analog and digital to function properly. Systems taking low-resolution analog measurements do not take readings that are precise enough to be impacted by coupled digital noise.

In systems sharing a ground plane, interaction between analog and digital ground return currents should be minimized. An analog component should not be placed between a digital component and its power supply because return currents traveling from the digital component across the ground plane can disturb the ground of the analog component.

In general, higher frequency digital components should be placed closer to the power supply than lower frequency components. If possible, each component should have a straight-line return path in a solid ground plane to the power supply ground.

1.2.5 Analog Measurement and Ground Noise

ADC measurements can be more precise by ensuring that the ground ADC voltage reference and the analog input circuit ground reference are at the same voltage. Differences in these two voltages are typically caused by asymmetrical current flowing in the ground plane past analog measurement circuits. Although in most embedded systems, designers connect the analog and digital ground planes near the PCB power supply, connecting the planes near the mixed-signal MCU can keep current flow symmetrical across the plane.

1.2.6 System Ground

A system of circuits or PCBs must return current to chassis ground or to the main power supply circuit ground. Noise can travel along this return path from one circuit to another. The effects of this kind of noise can be minimized by limiting the amount of interaction between the system's return currents [1]. Figure 1.8 Star Ground Topology on page 8 shows an example of this design technique called the star topology.

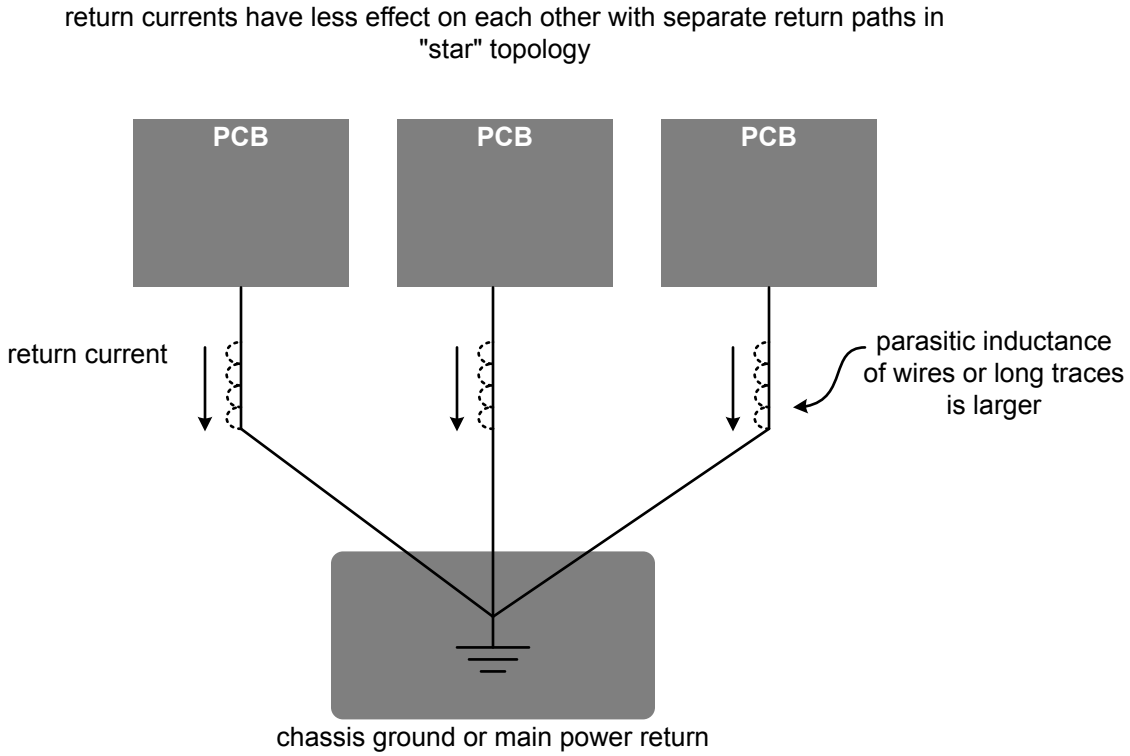


Figure 1.8. Star Ground Topology

2. Signal Traces

Mixed signal embedded systems carry both digital and analog signals across the PCB through strips of conductive metal. Just as radiated noise from digital can couple into the power and ground circuits, this noise can also couple into analog traces and degrade measurements. The following subsections discuss how placement and routing techniques of signal traces can minimize coupling.

2.1 General Guidelines

Digital and analog traces should be routed as far apart from each other as possible. Also, digital and analog traces should never be routed so that they are perpendicular to one another. High-frequency signals, such as the system clock or high-speed digital signals, radiate EMI due to reflections and differential mode currents in ground circuit conductors. At high frequencies, the trace-to-ground stray capacitance and parasitic inductances can detrimentally affect performance [5].

2.2 Trace Geometry and Impedance

An ideal trace would conduct any amount of current without any potential drop across the trace. In real-world systems, each trace has a characteristic impedance that depends on the following:

- Length.
- Thickness.
- Width.
- Distance from surrounding traces and ground planes.
- The material used in the PCB.
- Connections to the trace.

2.2.1 Trace Routing and Length

When routing signals, trace width should remain constant. Traces should be routed using two 45 degree turns instead of a single 90 degree turn, as shown in Figure 2.1 Trace Routing on page 9. Trace length should be kept at a minimum, as longer traces are more susceptible to EMI, and trace inductance and resistance increase as trace length increases.

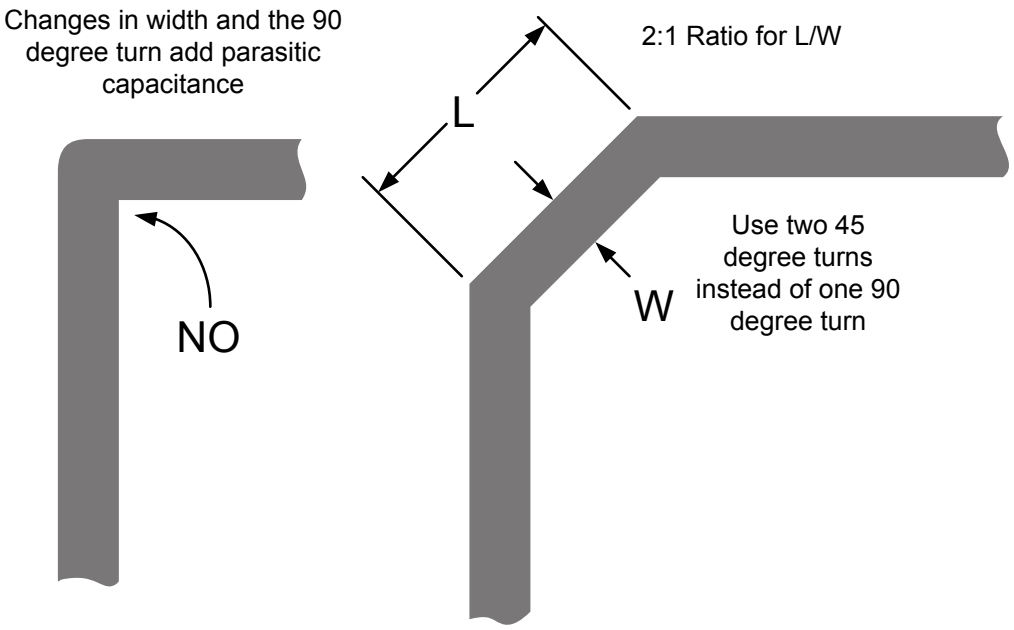


Figure 2.1. Trace Routing

2.2.2 Vias

When a signal must travel from one layer of the board to another, the trace must be routed through a via, which adds capacitance and inductance to a trace [7]. The via's capacitance shunts high-frequency components of signals to ground, which can round digital waveforms. The via's inductance can produce noise, reflections, and EMI. The use of vias should be minimized, especially in high-frequency traces.

2.2.3 Reducing Signal Trace Crosstalk

To minimize the effects of crosstalk, a phenomenon discussed in 9. Appendix C—Crosstalk, designers should follow the 3W Rule when routing high-frequency signals. The 3W Rule states that the separation between traces must be three times the width of these traces, measured from centerline to centerline [5]. This rule assumes that the traces are surrounded by a solid ground plane and are undisturbed by vias or cross-stitch traces.

2.2.4 Preventing Signal Reflection In Traces

At high frequencies, signal traces may act as transmission lines, and other traces can experience reflections [7] that can cause false triggering in digital logic, signal distortion, and EMI problems. The trace length at which reflections can become a problem is determined by the rise time of the signal traveling on the trace. Most microcontroller applications do not create reflections if traces are less than 100 cm.

3. Special Considerations

3.1 Unused Pins

Many embedded system designs do not use all available pins on a mixed-signal MCU. The following is a list of typical unused pin types and what action to take during PCB design:

- Digital general-purpose I/O port pins (GPIO)—Connect directly to digital ground and configured as open-drain with internal weak pull-lups disabled to save power, or they can be left floating and driven to logic 0 by software.
- Analog signals—Connect directly to analog ground, which reduces susceptibility to radiated noise.
- Op-amps—Connect their non-inverting (+) input to ground and the inverting input (-) to the op-amp output.

3.2 Special Signals

The following subsections describe design techniques for some critical and commonly used signals routed on PCBs.

3.2.1 System Clock

Traces connected to an external system clock carry a high-frequency signal and can radiate noise. To help keep system clock trace lengths minimal and reduce the amount of radiated noise, external oscillators should be kept as close as possible to the microcontroller. Noisy systems can radiate EMI and affect external system clock traces. When possible, designs should avoid the possibility of external clock source disruptions by using the internal oscillator. If a crystal oscillator is required in an application in which EMI susceptibility is a major concern, designs should use a canned CMOS oscillator that has its own power supply, ground, and amplifier. These metal can oscillators are less susceptible to disruptions caused by EMI than an exposed crystal oscillator.

3.2.2 Reset

Noise on the reset signal trace can cause inadvertent microcontroller resets. Noise on this line can be minimized by keeping the reset trace length short and by adding a decoupling capacitance of 1 µF. For additional noise immunity, add an external pull-up resistor of 1–10 kΩ to VDD. This pull-up is much stronger than the reset signal's relatively weak internal pull-up. If the reset is connected to other devices without an external pullup resistor, adding decoupling capacitance is still recommended. The reset signal should not be left unconnected, especially in electrically noisy environments. Figure 3.1 Decouple and Pull-Ups on the RSTb and MONEN Pins on page 12 shows an example of a reset circuit configuration.

3.2.3 VDD Monitor Enable (MONEN)

Some Silicon Labs MCUs feature a VDD monitor enable pin (MONEN). Tying this pin high to VDD enables the monitor, while tying it low to ground disables the monitor. This feature should always be enabled, except under special circumstances, such as specially-designed, low-voltage/low-power applications. Keep the trace between MONEN and VDD as short as possible to minimize the effects of coupled noise. The trace should be routed as far as possible from other electrically-noisy signal traces.

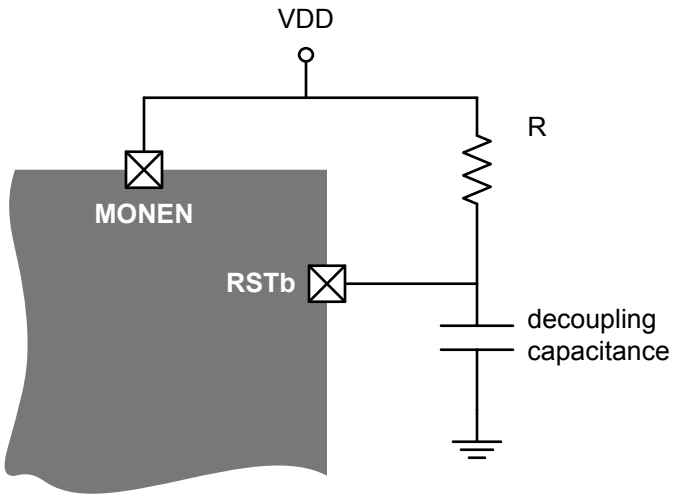


Figure 3.1. Decouple and Pull-Ups on the RSTb and MONEN Pins

3.2.4 Voltage References

For internal references that connect to a pin or external references, noise on voltage reference traces is seen by the microcontroller as noise in analog measurements. Placing a parallel capacitance of 4.7 µF and 0.1 µF close to the reference pins will decouple the signal and provide a low-impedance path to ground for high-frequency noise.

3.3 Debug Interface

The JTAG and C2 debug interfaces connect the PCB to off-board systems that are susceptible to coupling from external noise sources. The following subsections discuss design techniques that will minimize this susceptibility.

3.3.1 C2 Interface

"AN124: Pin Sharing Techniques" gives an in-depth discussion of C2 routing techniques. If the C2D and C2CK aren't used in the design, they should be treated as a normal port pin and RSTb, respectively. Application notes can be found on the Silicon Labs website: http://www.silabs.com/8bit-appnotes.

3.3.2 JTAG Interface

Because JTAG signals have only a weak on-chip pull-up resistance and are not deglitched, signal traces are particularly susceptible to noise coupling and EMI. To reduce EMI sensitivity, JTAG traces should be kept as short as possible. If the PCB is not galvanically isolated from the off-board equipment, the PCB and equipment must share a common ground, which can be established by connecting a pin of the JTAG header to the PCB ground plane.

The JTAG signals can be made more immune to noise by adding some passive circuitry. External pull-up or pull-down resistors can be added to aid the relatively weak on-chip pull-ups.

Most applications will be sufficiently protected by adding a 3–5 kΩ pull-up resistor to the TCK signal. If the device is to be used in a particularly noisy environment, all JTAG signals should have strong external pull-ups or pull-down circuits to digital ground. Note that placing a pull-down resistor on TCK will make the hardware incompatible with the USB Debug Adapter.

Capacitive ringing across long JTAG cables can cause communication difficulties. Placing a small series resistance on JTAG signals dampens this ringing and improve performance. Silicon Laboratories MCU target boards use a 5x2 header. Figure 3.2 JTAG Header on page 13 shows a circuit diagram for the header, along with connections for a JTAG device.

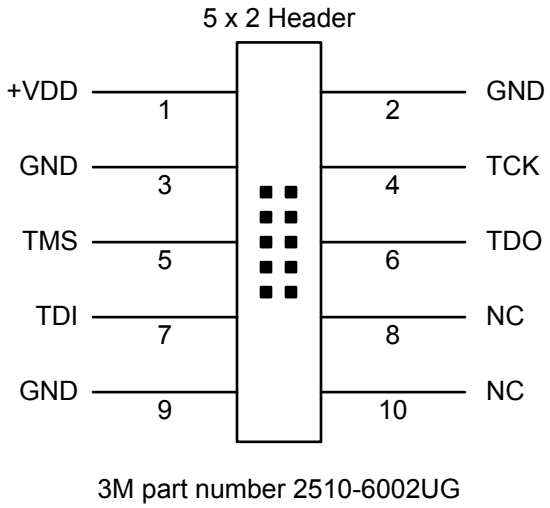


Figure 3.2. JTAG Header

4. Isolation And Protection

4.1 External Noise Sources

Traces routed to sources outside the PCB may experience electrical overstress (such as ESD), latch-up, and have a greater opportunity to share signals with systems that do not have the same ground potential. For a detailed discussion on latch-up, electrical overstress (or ESD), and ground loops, see 7. Appendix A—Rise Time-Related Noise.
Note: Several Silicon Labs MCUs (like the C8051F85x/86x family) have a GPIO that can be selected for use as an independent analog ground reference. Using this pin can greatly reduce the amount of PCB noise that is coupled into the ADC through either the input path or the reference path.

4.2 Prevention Techniques

A PCB can be protected from these noise sources using one or all of the techniques listed below [1] [5].

- Galvanic Isolation—Most commonly accomplished with optical isolation, which prevents ground loops and other ESD problems.
- Filtering—A series resistor or inductor limits the amount of current that an electrical overstress or ESD event can force into the PCB, while a shunt capacitance gives high-frequency noise a low-impedance path to ground.
- Transorbs or Schottky Diodes—These components act to divert high current to power or ground to prevent electrical overstress or ESD damage to the device. They also aid in preventing a latch-up condition.

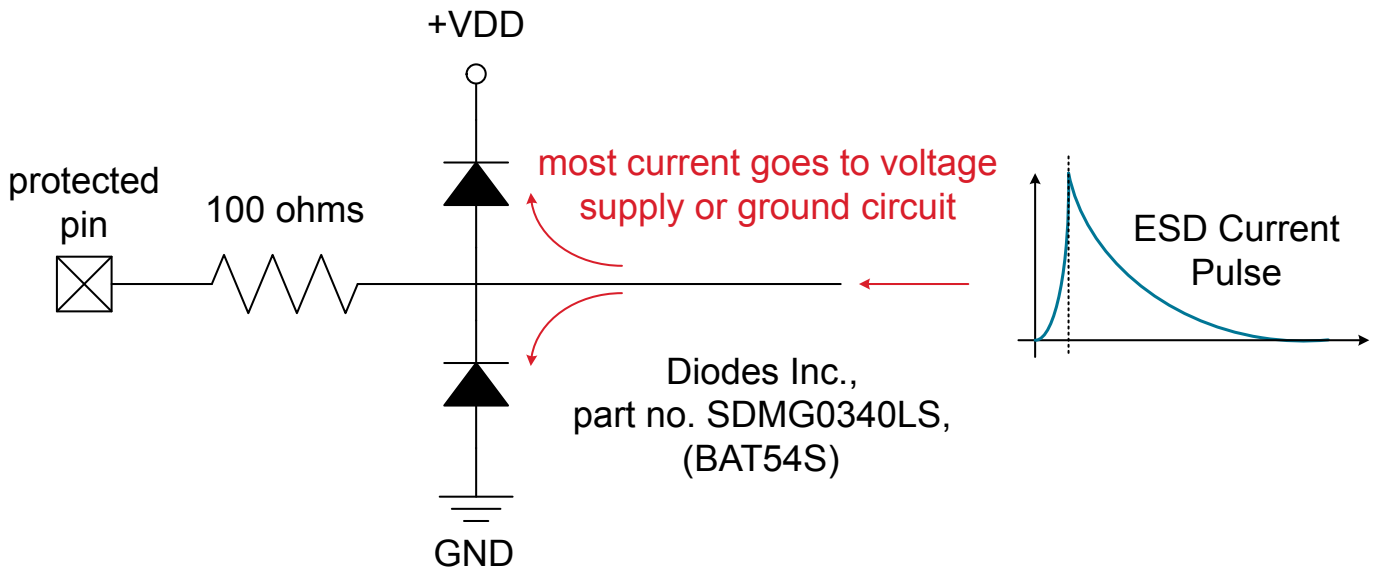


Figure 4.1. Example ESD/Latchup Protection Circuit

Diodes can be used when a PCB's signal trace interfaces with an external component with dissimilar power and ground voltage supply levels. One diode should be connected from the signal trace to the voltage supply, and another should be connected from the trace to ground. To ensure that the majority of current is diverted to power or ground and not through the protected device, an in-series resistance on the signal trace should be used in conjunction with the diode.

4.3 Industrial Systems

Noisy or industrial environments should always be electrically isolated from embedded system PCBs. Industrial systems can potentially present damaging events to a PCB. By employing the power, ground, and signal isolation and protection methods discussed in the previous sections, a PCB will be much less susceptible to all the detrimental effects of a noisy system.

5. Multilayer Board Design

In lower-frequency applications with few components, all signal routing and components can be placed on a two-layer board. However, many PCB designs can best be implemented using a board with multiple layers for components, signals, power, and ground. Multilayer boards allow the used of ground and power planes to reduce noise and EMI emissions and allow greater flexibility in the proper routing and placement of signal traces.

5.1 Benefits and Disadvantages of Multiple Layers

Below is a list of several factors that should be considered when determining the number of layers used in the design of a PCB.

- Routing Concerns—Adding layers offers more flexibility in trace spacing and placement to prevent crosstalk and noise coupling, especially in mixedsignal designs that have both analog and high-speed digital signals.
- EMI Control—Ground and power planes aid in the coupling of high-frequency return currents to their traces and reduce emissions.
- Noise Reduction—Low impedance ground and power planes reduce noise in digital and analog circuits.
- Cost—Adding layers to a PCB increases the cost of manufacturing the board.

5.2 Layer Types

Many designs use a signal plane on the component side of the board, and a ground plane on the other. Most PCBs today have a solid ground plane. Many designs also use a power plane (as opposed to power traces) to supply power to resident ICs. Power and ground planes are also referred to as image planes, as they help to couple signals to their traces, reducing common-mode RF currents as well as EMI emissions. In addition, ground fill and ground/power planes improve the thermal dissipation properties of PCBs. As a general rule of thumb, the more copper in the board, the better.

5.3 Layering Guidelines

The rules discussed in 2. Signal Traces can also be applied to designs with power and ground layers.

- Split analog and digital ground layers should still be connected at just one point. They should not overlap each other in different layers.
- High-speed digital signal traces should be routed over the digital plane, and analog signals should be routed over the analog plane.
- Component placement should follow the same guidelines discussed in 2. Signal Traces.

Designers must also be mindful of layer placement. All signal layers should be placed adjacent to image planes to provide a low-impedance path for RF return currents. For optimal EMI suppression, higher speed and critical trace signal layers should be adjacent to a ground plane and not adjacent to a power plane [5].

See Figure 5.1 Four-Layer Board on page 16, Figure 5.2 Six-Layer Board on page 16, and Figure 5.3 Eight-Layer Board on page 17 for recommended layer configurations. For further reference, the texts, “Printed Circuit Board Design Techniques for EMC Compliance” [5:17] and “High Speed Digital Design” [7], make recommendations for the way layers should be arranged.

Figure 5.1. Four-Layer Board

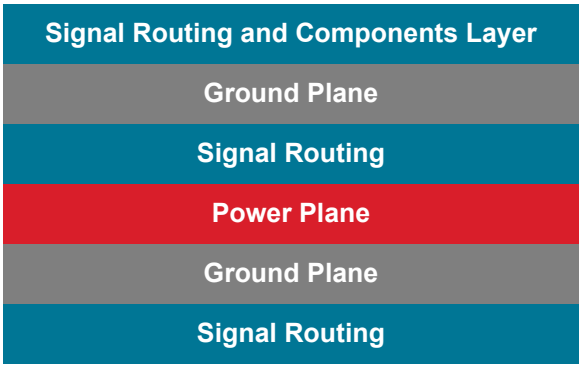


Figure 5.2. Six-Layer Board

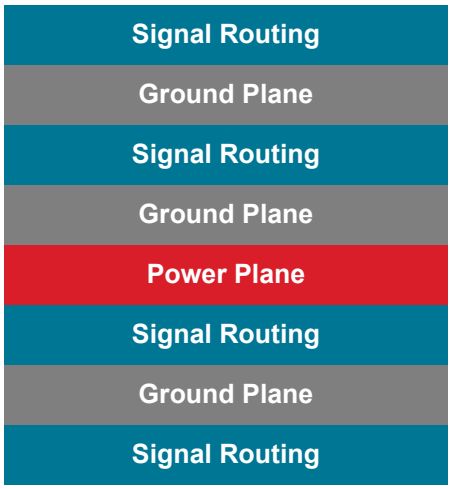


Figure 5.3. Eight-Layer Board

6. Design Checklist

6.1 PCB Testing

- Test your PCB design using prototype boards.
- Add jumpers that can connect traces and planes on prototype boards to aid testing of ground plane connections, power supply nets, etc.
- Design with a place to add bypass capacitors so that different capacitances can be tested in order to find the optimal value.

6.2 Power Supply Circuit

- Filter the output of dc-dc converters by adding bypass capacitance to the converter's output.
- Add a large bulk capacitor at the voltage regulator's output that can provide current for local capacitors and ensure regulator stability.
- Place bulk capacitors as close to the voltage regulator output as possible.
- The large bulk capacitor's capacitance should be 10 to 100 times as large as local IC decoupling capacitors.
- Tantalum and electrolytic capacitors work well as bulk decoupling capacitors.
- Add a second capacitor an order of magnitude or two smaller in capacitance relative to the large bulk capacitor to help filter high-frequency noise.
- Place a local capacitance as close as possible to the power supply pin of each IC.
- The side of the local capacitor that connects to ground should be placed as close to the IC's ground pin as possible in order to minimize the loop area between the cap and the power and ground pins.
- Add a filter, such as an L-C filter or an R-C filter, to the power supply circuit.
- Filter the analog voltage supply using a series inductance, either in the form of a ferrite bead or a 2 Ω wire-wound resister.

6.3 Ground

- Design using a ground plane instead of traces connecting components to ground.
- The ground plane should cover as much of the board as possible, including the spaces between devices, traces, and the area underneath the mixed-signal MCU.
- Separating the analog ground plane from the digital ground plane improves analog performance.
- Separate ground planes should be connected in only one location, usually close to the power supply.
- Connecting separate ground planes near the microcontroller instead of the power supply can sometimes improve analog performance.
- If possible, place the mixed-signal MCU over the analog ground plane. Otherwise, try to place the device so that the analog-related pins reside over the analog ground plane.
- An analog component should not be placed between a digital component and the power supply.
- Be mindful of return current paths for all components.
- If possible, each component should have a straightline return path in the solid ground plane to the power supply ground.
- Isolate the PCB's ground plane from noisy systems' ground circuits.

6.4 General Guidelines

- Keep analog and digital signals as far apart from each other as possible.
- Avoid routing analog and digital traces perpendicular to each other.
- Trace width should remain constant throughout the length of the trace.
- Turns in traces should be routed using two 45 degree turns instead of one 90 degree turn.
- Trace length should always be minimized.
- Use vias only when absolutely necessary.
- Avoid the use of vias when routing high-frequency signals.
- Follow the 3W Rule, which states that the distance between adjacent traces should be equal to two trace widths when routing signals close to each other.
- Keep traces less than 100 cm to minimize reflections.

6.5 Special Considerations

- Connect unused I/O pins to ground, and configure them as open drain with weak pull-ups disabled. Alternatively, leave them unconnected and drive them to logic low.
- Connect unused analog signals directly to analog ground.
- Connect unused op-amp's non-inverting (+) input to ground and the inverting input (–) to the op-amp output.
- When possible, use the microcontroller's internal oscillator.
- If an external oscillator must be used, consider using a canned CMOS oscillator that has its own power supply, ground, and amplifier if the system will be used in an electronically-noisy environment.
- Place the external oscillator as close as possible to the microcontroller.
- Keep the reset signal's trace length as short as possible.
- Add a decoupling capacitance of 1 µF and an external pull-up resistor of 1–10 kΩ between VDD and the reset pin.
- Never leave the reset signal floating in noisy environments.
- Keep the trace length of the VDD monitor signal as short as possible, and route this trace as far as possible from electrically-noisy signal traces.
- Place a parallel capacitance of 4.7 µF and 0.1 µF close to the voltage reference pins.
- See "AN124: Pin Sharing Techniques for the C2 Interface" for details concerning C2 interface layout techniques.
- If the C2 interface pins, C2D and C2CK, will not be used in the design, treat them as the normal port pin and reset pin, respectively.
- Keep JTAG traces as short as possible.
- Either galvanically isolate JTAG ground from offboard equipment or make sure that the PCB and the off-board equipment share a common ground.
- Add a 3–5 kΩ pull-up resistor to the JTAG interface's TCK pin to reduce susceptibility to EMI.
- In noisy systems, add pull-down or pull-up resistors to every JTAG signal.
- Place small series resistance on JTAG traces that are routed to external connectors.

6.6 Isolation And Protection

- Isolate PCB circuits from external systems by galvanic isolation, filtering, or circuits with transorbs or diodes.
- Diodes can be used when a PCB's signal trace interfaces with an external component with dissimilar power and ground voltage supply levels.
- Use a series resistance on the signal trace in conjunction with the diode.

6.7 Multilayer Designs

- Design using a power plane instead of traces routed from the power supply.
- Connect split analog and digital ground layers at just one point.
- High-speed digital traces should not jump layers because these signals radiate the most noise from vias.
- Place all signal layers adjacent to image planes.
- Place higher speed and critical trace layers adjacent to ground layers and not power layers.

7. Appendix A—Rise Time-Related Noise

7.1 Introduction

The period of time required for a signal to transition is known as its rise time. Digital logic gate switching during this rise time results in high-frequency noise. The faster the typical logic gate transition time, the higher the range of frequency band of interest. Figure 16 shows the area of a digital waveform where the signal is transitioning from one state to the other.

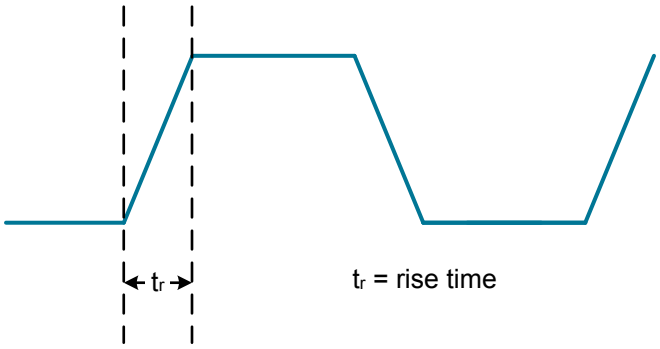


Figure 7.1. Digital Waveform Rise Time

This bandwith can be determined by:

$$BW = \frac{1}{\pi \times t_r}$$

Silicon Labs devices' digital signals have a typical rise time of 200 ps. Using this equation, the calculated bandwidth of interest is approximately 1.6 GHz down to the system clock's fundamental frequency. To minimize noise, impedance along the trace within this bandwidth should be kept to less than 10 Ω.

7.2 Relationship between Current Draw and Voltage Change

At high frequencies, the inductance of traces causes them to have high impedances, and rapid changes in current cause unwanted voltage changes that can affect all devices sharing that voltage supply. The following equation shows the relationship between a change in current, a change in voltage, and the trace's characteristic impedance. Characteristic Impedance (Z_0) dictates the change in voltage for a given change in current.

$$dV = dI \times Z_0$$

The characteristic impedance of a trace is a function of the trace inductance, capacitance, series resistance, and shunt conductance [4]:

$$Z_0 = \sqrt{\frac{R_{series} + L_t}{G_{shunt} + C_t}}$$

For the purposes of illustration, assume the trace is ideal (i.e., lossless) where R_{series} and G_{shunt} are zero, which reduces the equation to [1]:

$$Z_0 = \sqrt{\frac{L_t}{C_t}}$$

7.3 Lowering Impedance through Decoupling

The characteristic impedance can be lowered by either lowering the inductance or by increasing the capacitance of the circuit. Because of the difficulty of lowering inductance in a circuit, most designs add capacitance instead. This capacitance should be connected to the voltage supply trace and to the device's ground circuit; this method is referred to as decoupling.

As was discussed in 1.1.2 Power Supply Bulk Decoupling and Bypassing, a bulk decoupling capacitor provides a current reservoir for decoupling capacitors local to each IC. The impedance of each local decoupling and bypassing loop must be lower than the impedance of the main voltage supply loop. If it is not, the bypassing function of the local capacitive loop will not be effective.

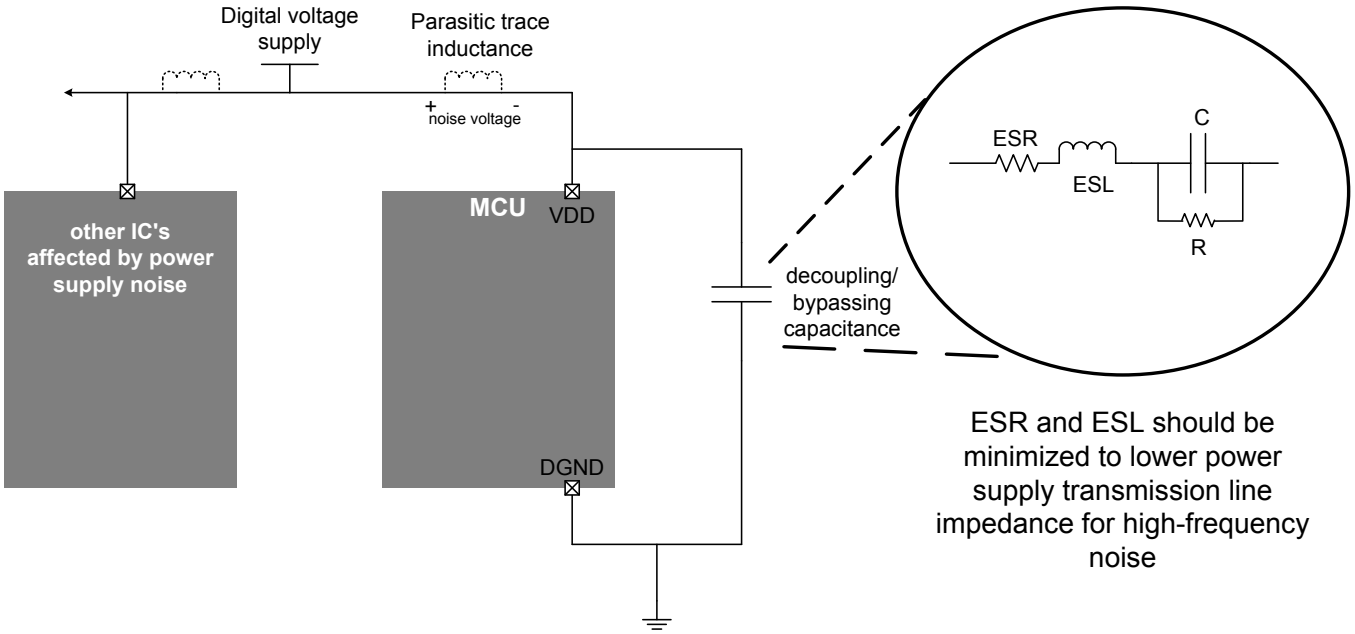


Figure 7.2. Local Decoupling and Bypassing Circuit

8. Appendix B—Capacitor Choice and Use

8.1 Introduction

For optimal PCB performance, designers must carefully select the correct type of capacitor for the task. Capacitors vary in terms of temperature coefficient, dielectric constant, dielectric absorption, voltage ratings, effective series resistance (ESR), effective series inductance (ESL), etc. The following sections provide a detailed exploration of capacitor behavior and characteristics.

8.2 Non-Ideal Capacitor Behavior

At high frequencies, the ESL of a capacitor becomes dominant, and the capacitor's impedance actually increases as frequency increases. Since decoupling and bypass capacitors should have low impedances at high frequencies, capacitors used for these purposes should have low ESL. Ceramic or metallized film are the two most commonly used capacitors for decoupling and bypassing. Also, surface mount capacitors introduce less inductance to a circuit than through-hole capacitors.

Every capacitor has a self-resonant frequency determined by the series capacitance and the lead inductance. The resonant frequency of the chosen capacitor should be greater than five times the fundamental system clock frequency in order for the capacitor to be useful for decoupling. The following equation shows the relationship between the characteristics of a capacitor and its impedance relative to frequency [7].

$$X(f) = \left(\mathrm{ESR}^2 + \left(\frac{-1}{2\pi f C} + 2\pi f \mathrm{CL}\right)^2\right)^{1/2}$$

8.3 Ceramic Capacitor Types

The best ceramic capacitors use either C0G, a Z5U, or a X7R dielectric. C0G dialectrics are the best (and the most expensive). Between X7R and Z5U, a Z5U dielectric has lower temperature stability but a higher dielectric constant, which means that a smaller package size can provide more capacitance, but the capacitance will vary across the industrial temperature range.

Conversely, an X7R dielectric has better temperature stability but a lower dielectric constant. X7R dielectrics also have less dielectric loss than Z5U above their respective self-resonant frequencies.

X7R is generally available, cost effective, and functional for the capacitance range needed for decoupling and bypassing. For bulk decoupling, which requires higher capacitance, tantalum electrolytic capacitors are commonly used in conjunction with a smaller X7R or Z5U ceramic capacitor.

8.4 Capacitor Values

A PCB design should use the smallest capacitor values possible while still providing adequate decoupling. The high-frequency digital signals of Silicon Laboratories' MCUs are best decoupled by using small capacitance with low ESL. If several devices share the same power supply circuit and all components share the same ground plane, place a 100 pF and a 0.01 µF capacitor in parallel as close to the MCU voltage supply pin as possible for bulk decoupling and bypassing. Larger capacitance values can be used if the power supply powers only the MCU devices, or if the system uses separate digital and analog ground planes.

The designer should experiment with different capacitor values and types if noise reduction is critical in the design. For further reference, see [7:274, 281]. Reference [7] gives straightforward methods of calculating effective impedances and provides notes on capacitor value choices.

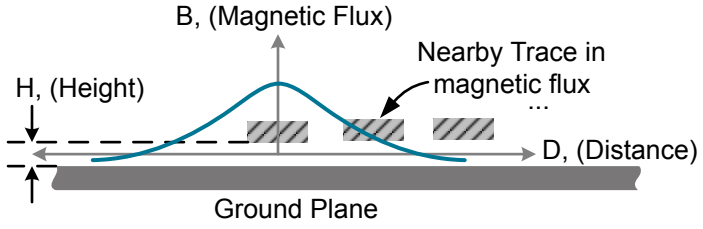


Figure 8.1. Magnetic Flux as a Function of Distance from a Trace

9. Appendix C—Crosstalk

9.1 Introduction

Signal traces and their corresponding ground circuits carry time-varying currents that create magnetic fields. These fields radiate EMI to surrounding components and can also induce electrical noise in nearby traces [5] [7]. As current flow increases and decreases through a trace, an equal amount of current must return through the ground circuit, most often through the ground plane. Because other traces share this ground plane, current transients on one trace affect other traces. This effect is commonly called crosstalk.

The magnetic flux due to current change in a trace (B in Figure 18) can induce voltage changes in nearby taxes. This effect decreases as a function of the square of the distance-to-height ratio, (D/H)2 [7]. Crosstalk also increases with increased trace length and signal risetime (K). The 3W Rule minimizes crosstalk by ensuring that adjacent traces are sufficiently far apart to avoid being affected by magnetic flux.

$$\text{Crosstalk} = \frac{K}{1 + \left(\frac{D}{H}\right)^2}$$

10. Appendix D—Damaging Electrical Events

10.1 Latchup and ESD

Often an input to a CMOS device comes from another device with a different power supply voltage. If the CMOS device is not powered before the connected input device is powered up, a short can be created across the port pin's logic between the CMOS device's power supply and the ground pin. This event is commonly called latchup and can destroy a CMOS device. Figure 10.1 Example Latchup Potential on page 25 shows a circuit that is susceptible to latchup and indicates the point in the circuit where protection can be added.

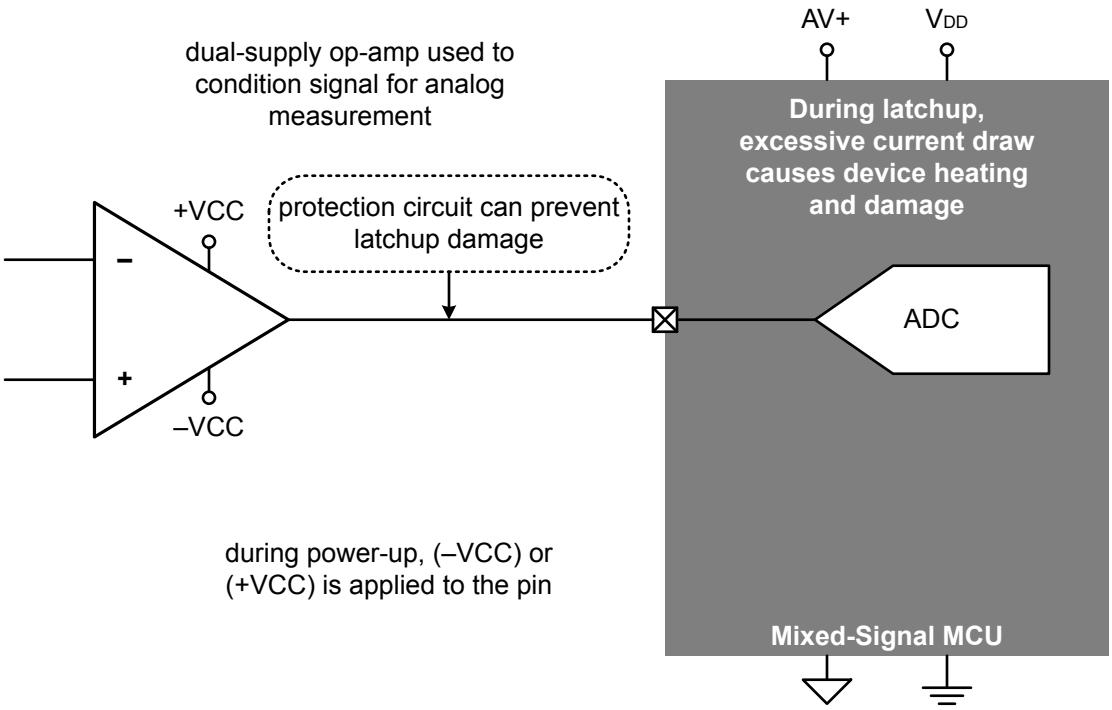


Figure 10.1. Example Latchup Potential

Electrostatic Discharge (ESD) on a CMOS device pin can force the device out of its specified voltage range and damage the device. ESD can appear as a surge of voltage originating outside the PCB that couples into a signal trace. ESD can also induce CMOS latch-up. Figure 12 shows the protection circuit that can prevent ESD or latchup event damage. Ground loops occur whenever connected circuit boards do not share a common ground, as shown in Figure 10.2 Ground Loop Created by Multiple Ground Connections on page 26. Ground loops can cause noise, damage, or injury.

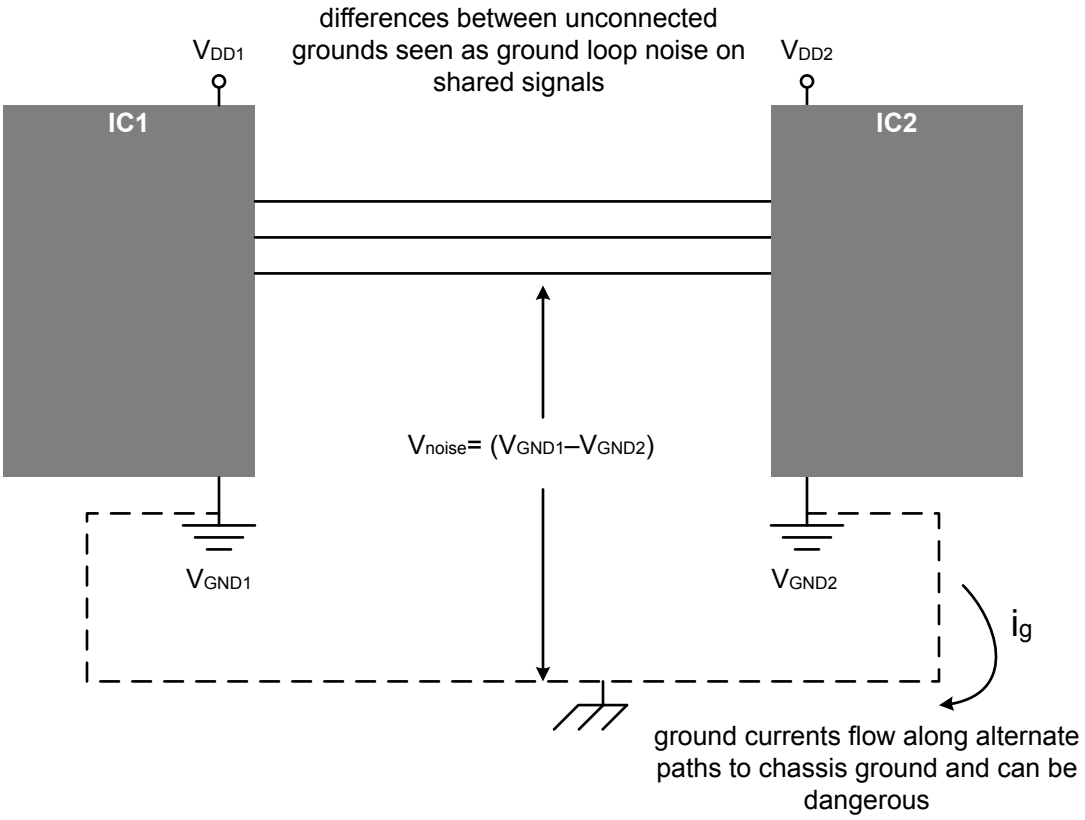


Figure 10.2. Ground Loop Created by Multiple Ground Connections

10.2 Preventing Ground Loops

To prevent ground loops, galvanically isolate interfacing boards, as shown in Figure 10.3 Ground Loop Prevention on page 27. Isolation can be accomplished through the use of optical isolators, transformers, and common-mode chokes. Most isolation devices are not linear and, therefore, introduce some amount of distortion, which can affect analog performance.

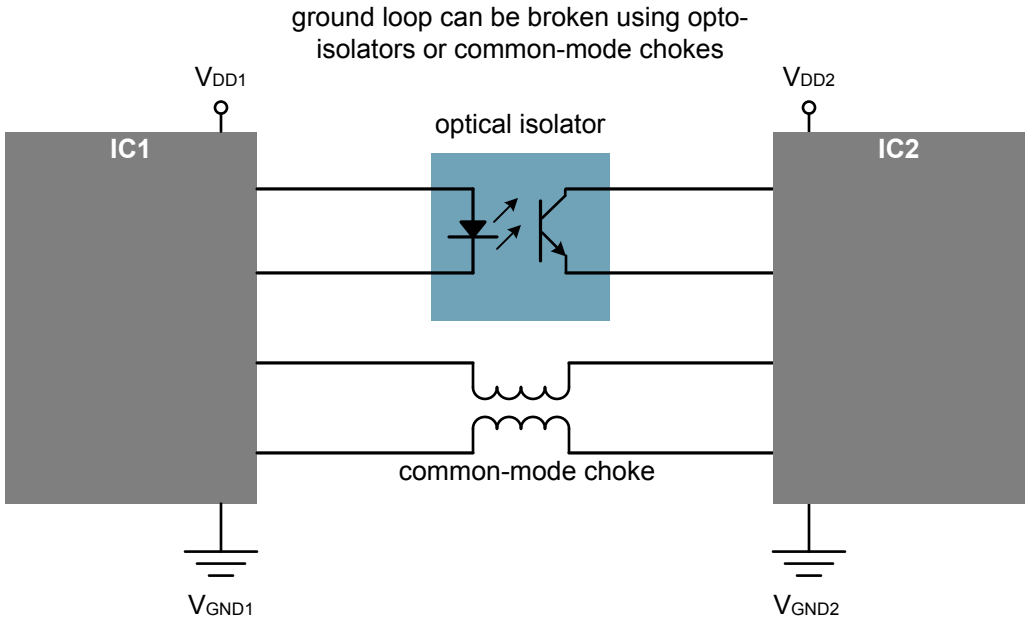


Figure 10.3. Ground Loop Prevention

Ground loops can also be prevented by connecting each system to a common ground connection, as shown in Figure 10.4 Preventing Ground Loops by Sharing a Common Ground on page 27. This ensures that every system has the same ground potential. Reference [1] provides more information on ground loops and prevention.

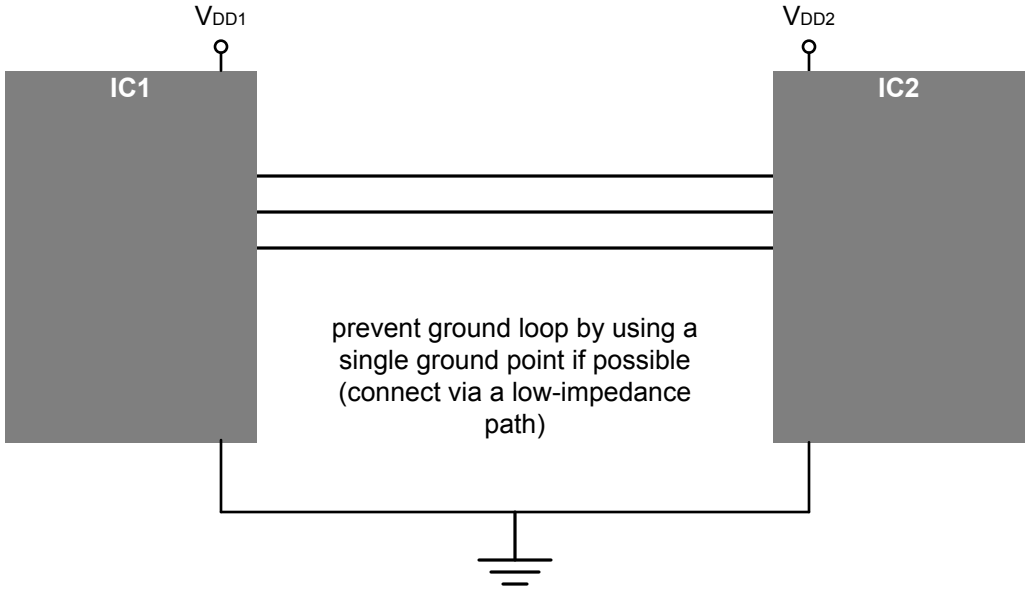


Figure 10.4. Preventing Ground Loops by Sharing a Common Ground

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