AN1341: RS9116 CC0 Board Layout Guidelines

Version 1.1

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1 Introduction

This Application Note provides PCB layout guidelines for the RS9116 CC0 SiP module. These guidelines cover parts placement, various critical traces routing like RF, and host interfaces routing like SDIO/SPI, USB, UART, Power Routing and GND Pour. CC0 module placement and routing can be done within a 4-layer PCB stack-up. However, designers can choose higher number of layers, based on product needs. This document describes placement and routing considering a 4-layer stack-up setup.

Below is the recommended layer stack-up and placement/routing considering a 4-layer stack-up. Exact PCB thickness can be as per the layer stack-up provided by the PCB manufacturer. It is recommended to use a PCB thickness close to 1.6 mm, but designers can choose suitable thickness based on product needs.

- Layer 1 : Parts Placement, RF circuitry, Interface signals (SDIO/SPI, USB, UART)
- Layer 2 : GND
- Layer 3 : Power supply star routing
- Layer 4 : Power supply star routing, UART Interface signals and GPIOs

2 Placement Guidelines

Designers can choose suitable antenna as per the product needs, like Chip, on-board PCB trace, External PCB trace, Dipole, etc. In this Application Note, a Chip antenna is considered on RF_PORT2 pin of the module, and a U.FL connector (for an external antenna) is considered on RF_PORT1 pin. However, designers can choose any antenna on any RF port based on product needs.

Here are the recommendations for the placement of the CC0 module and its associated parts. Parts are placed on the same side of the CC0 module, in this document. However, designers can choose to place them on either side of the PCB to achieve best placement and routing. The steps below can be sequentially followed to achieve optimal placement.

1. To get the best RF performance from the CC0 circuitry and antenna, it is recommended to place antenna circuitry near the PCB edge. Antenna part guidelines must be followed for its placement and routing.
2. Place the RF components, antenna, and the CC0 module on the same side of the PCB, so that there are no vias on RF traces.
3. RF front-end components and the CC0 module should be placed with minimal distance from RF_PORT pin on the module till the antenna, so that RF traces lengths are as short as possible.
4. Decoupling capacitors are recommended to be placed on intended power pins. Decaps must be placed within 5 mm distance from the module pins.
5. VINBCKDC Capacitor should be placed within 10 mm distance from the module pin.
6. Buck Inductor should be placed within 5 mm distance from VOUTBCKDC pin. Buck capacitor should be placed within 1 mm distance from the Buck Inductor.
7. Series resistor on Clock signal of SPI or SDIO interface, must be placed close to the source of this clock signal. It must not be placed near the module end of the signal.

Considering the above recommendations, the CC0 module and its circuitry can be placed on the single side of PCB as shown below. This takes 25 mm x 15 mm of board space approximately, until RF front-end discrete components. Designer can choose to place the components different from the below recommendation to suit the product needs.

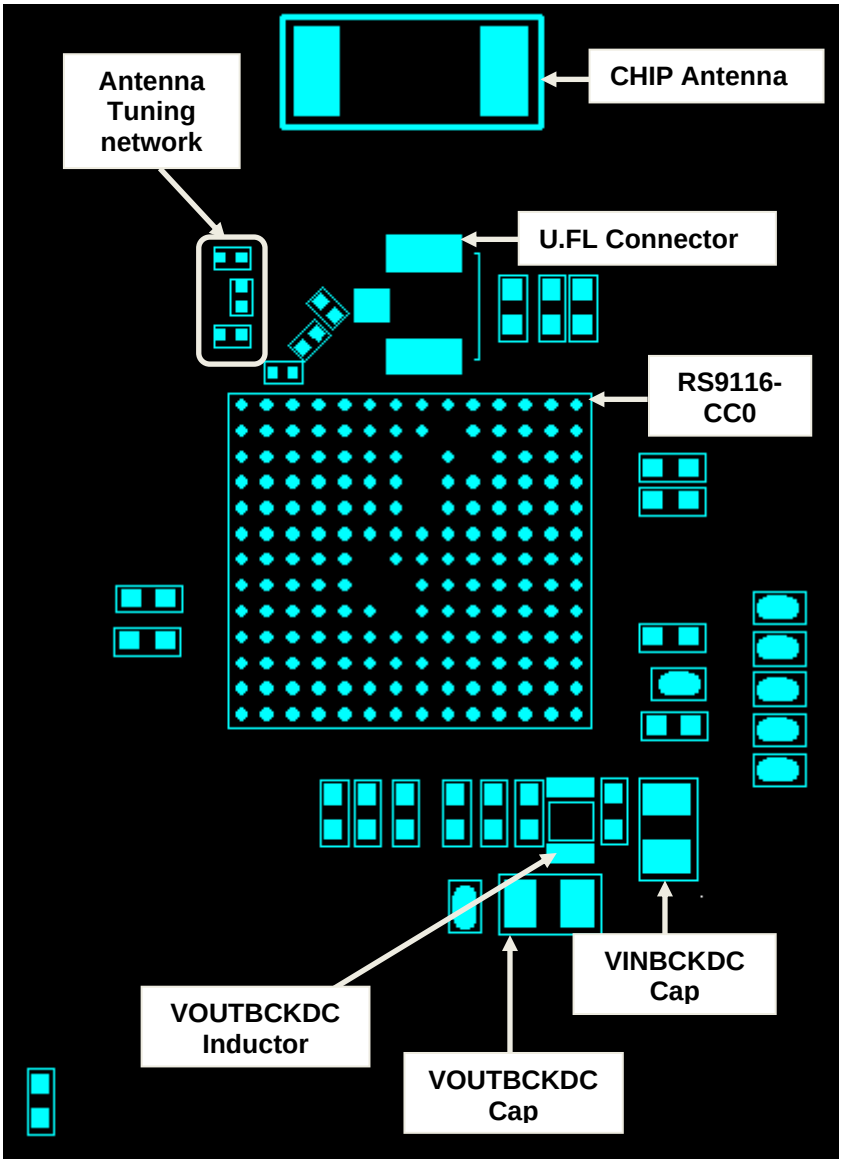

Figure 1: CC0 Module and Components Placement

3 RF Layout Guidelines

RF parts placement and traces routing affect the RF performance of the module and circuitry. Great care must be taken to ensure best design practices and below guidelines are followed.

1. The RF trace on RF_PORT1and RF_PORT2 should have a characteristic impedance of 50 Ω. Any standard 50 Ω RF trace (Micro-strip or Coplanar wave guide) may be used. The width of the 50 Ω line depends on the PCB stackup, e.g., the dielectric of the PCB, dielectric constant of the material, thickness of the dielectric, and other factors. Consult the PCB fabrication unit to get these factors right.
2. There must be DC blocking capacitors (8.2 pF) on RF_PORT2 and RF_PORT1 if they are connected to antenna.
3. A thicker trace allows more manufacturing tolerance while keeping 50 Ω impedance.
4. Keep the length of the RF traces as short as possible.
5. Route the RF traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
6. Maintain at least one trace-width of space between nearby GND pour and the RF trace.
7. Add GND stitching vias around RF traces.
8. Do not route any digital or analog signal traces between the RF traces and the reference ground.
9. Etch the GND copper underneath the antenna in all layers.
10. Follow the antenna placement as per the antenna vendor layout guidelines.
11. To evaluate transmit and receive performance like TX Power and EVM, RX sensitivity and the like, an RF connector would be required. Since the antenna is connected to the RF_PORT2, connect the U.Fl connector to the RF_PORT1 for RF related test and evaluation.
12. The RF_PORT2 (module pin no. N14) signal may be directly connected to an on-board chip antenna or terminated to an RF connector of any form factor for enabling the use of external antennas.
13. Use ground pour on the top and bottom layers in the RF area with plenty of ground stitch vias. Use stitching in a staggered pattern with a minimum via spacing of 32 mil (via to via, 25-mil offset) and a maximum spacing of 100 to 150 mil. After ground flooding, terminate shapes and corners with vias to tie to other planes for improved EMI performance.
14. Etch the GND fill underneath the U.FL connector on top layer.

Considering the above recommendations and the placement guidelines described in the earlier section, possible RF circuitry routing in Layer 1 is shown below. Major parts and traces are also highlighted below.

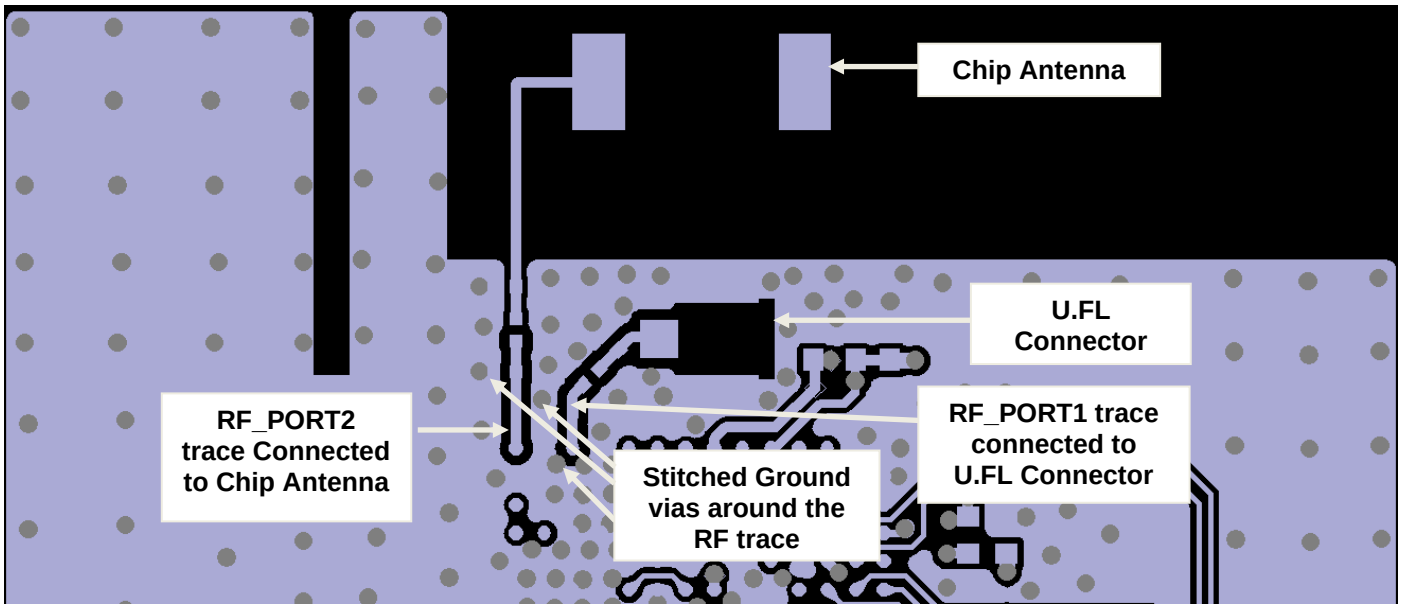

Figure 2: RF Circuitry Routing in Layer 1

The image below shows the overlap of RF routing on Top layer and the GND plane in the second layer. As can be observed, entire RF circuitry has the Layer 2 as GND reference. GND vias around RF circuitry are stitched directly to the GND plane.

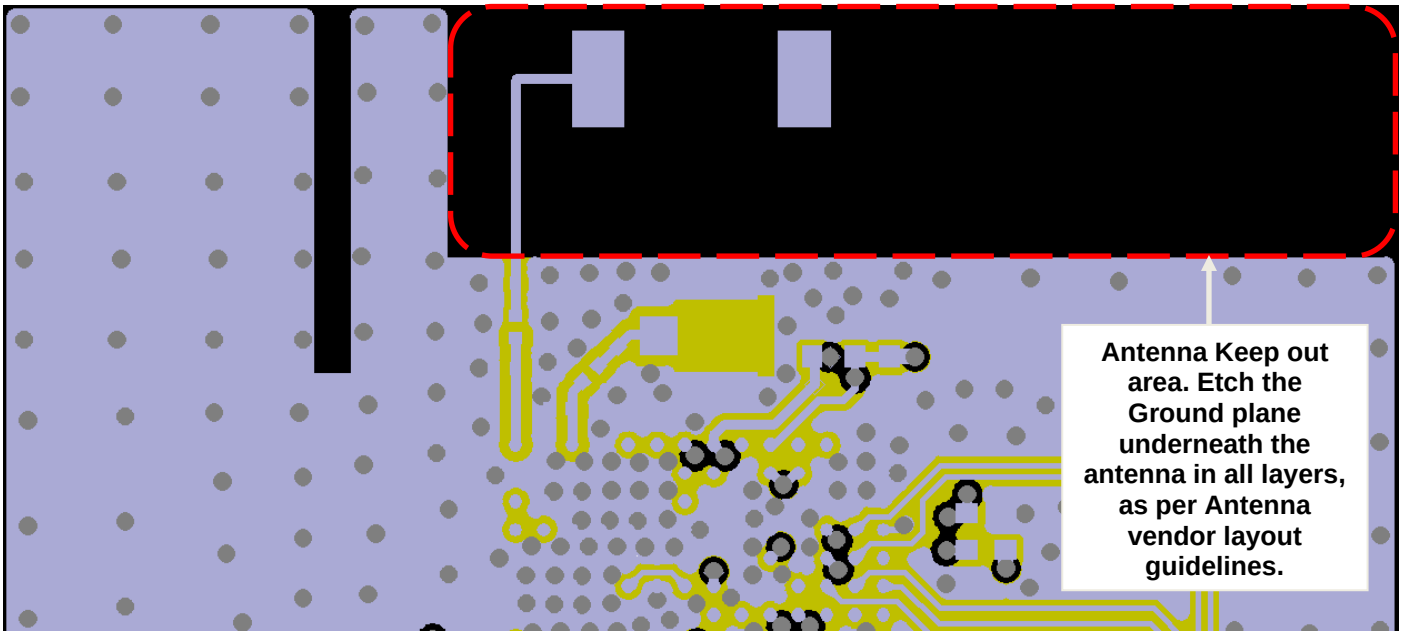

Figure 3: RF Circuitry Overlap with GND Layer

4 SDIO/SPI Layout Guidelines

SDIO and SPI are high speed interfaces where-in clock signals can reach up to 100 MHz. High speed design guidelines like below must be followed for the signals in these interfaces. SDIO/SPI signals include SDIO_CLK/SPI_CLK, SDIO_CMD/SPI_CSN, SDIO_D0/SPI_MOSI, SDIO_D1/SPI_MISO, SDIO_D2/SPI_INTR, SDIO_D3.

1. The Characteristic impedance of the SDIO/SPI lines should be 50 Ω.
2. Match the lengths of all SDIO/SPI lines within 100 mils tolerance.
3. Keep the SDIO_CLK/SPI_CLK trace away from nearby traces with minimum 2x distance.
4. Do not route any parallel traces above or underneath the SDIO_CLK/SPI_CLK trace.
5. Keep SDIO/SPI traces away from all clock lines and noisy power supply components such as the switcher inductors. Avoid crossing over power supplies or ground discontinuities. SDIO/SPI traces must have a solid ground on the layer adjacent to them.
6. Do not leave any stubs on the SDIO/SPI traces.

The image below shows the SDIO/SPI traces routing in Layer 1, as an example. The series resistor on SDIO_CLK/SPI_CLK is placed closer to the source of this clock, rather than placing closer to the CC0 module.

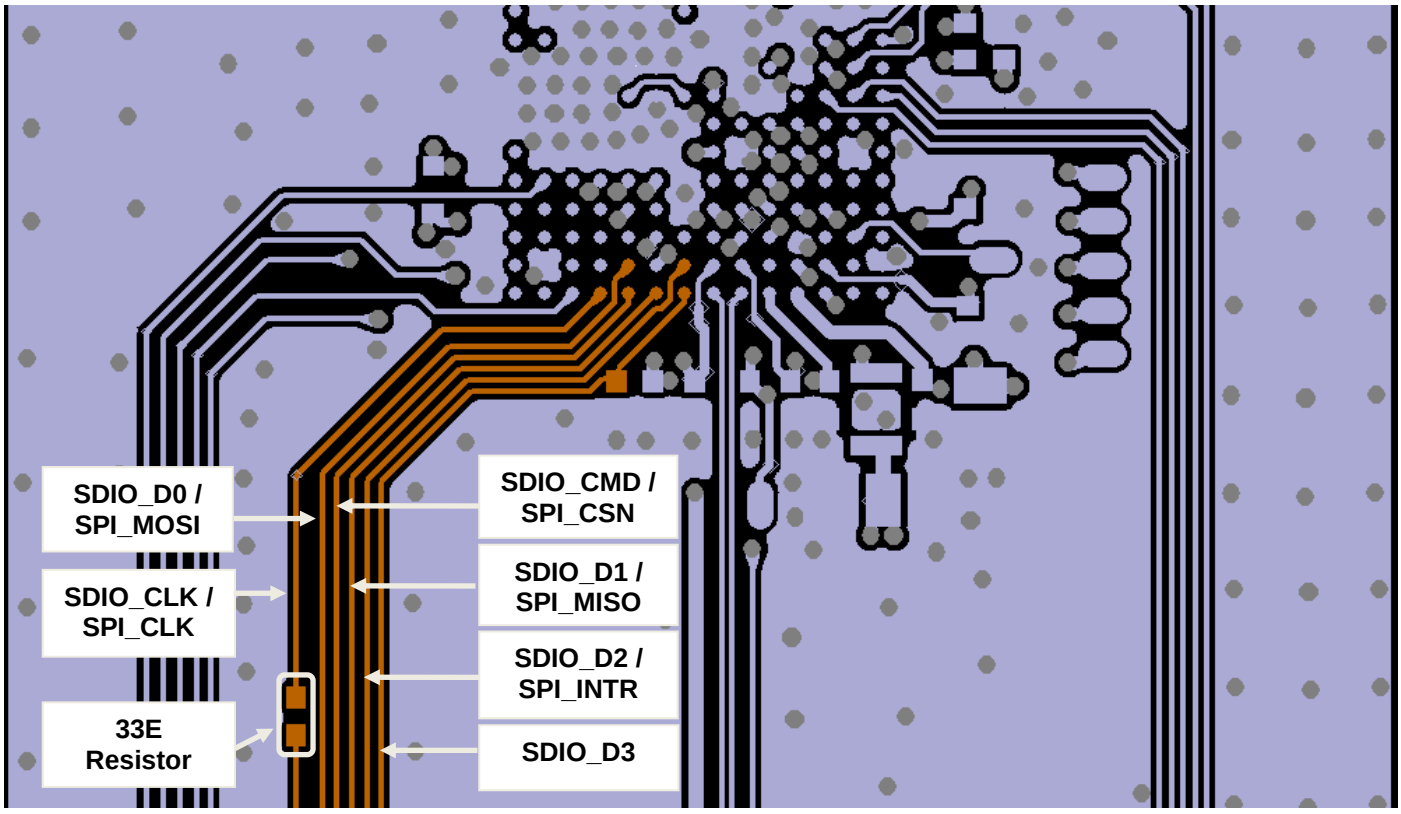

Figure 4: SDIO/SPI Signals Routing in Layer 1

5 USB Layout Guidelines

USB signals can reach speeds of 480 Mbps. Guidelines for the differential signals USB_DP and USB_DM must be followed.

1. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (i.e., a) that achieves 90 Ω of differential impedances and 45 Ω for each trace.
2. To minimize crosstalk between the two USB differential signals (USB_DP and USB_DN) and other signal traces routed close to them, it is recommended that a minimum spacing of 3xa be maintained for low-speed non-periodic signals and a minimum spacing of 7xa be maintained for high-speed periodic signals.
3. It is recommended that the total trace length of the signals between RS9116 part and USB connector (or USB host part) be less than 450 mm.
4. If the USB high-speed signals are routed on the top layer, best results will be achieved if Layer 2 is a continuous GND plane. Furthermore, there must be only one ground plane under high-speed signals and avoid the high-speed signals crossing from one GND plane to another GND plane.
5. Do not route the USB differential lines close to edge of the board.

The image below shows USB differential traces routing in Layer 1, as an example.

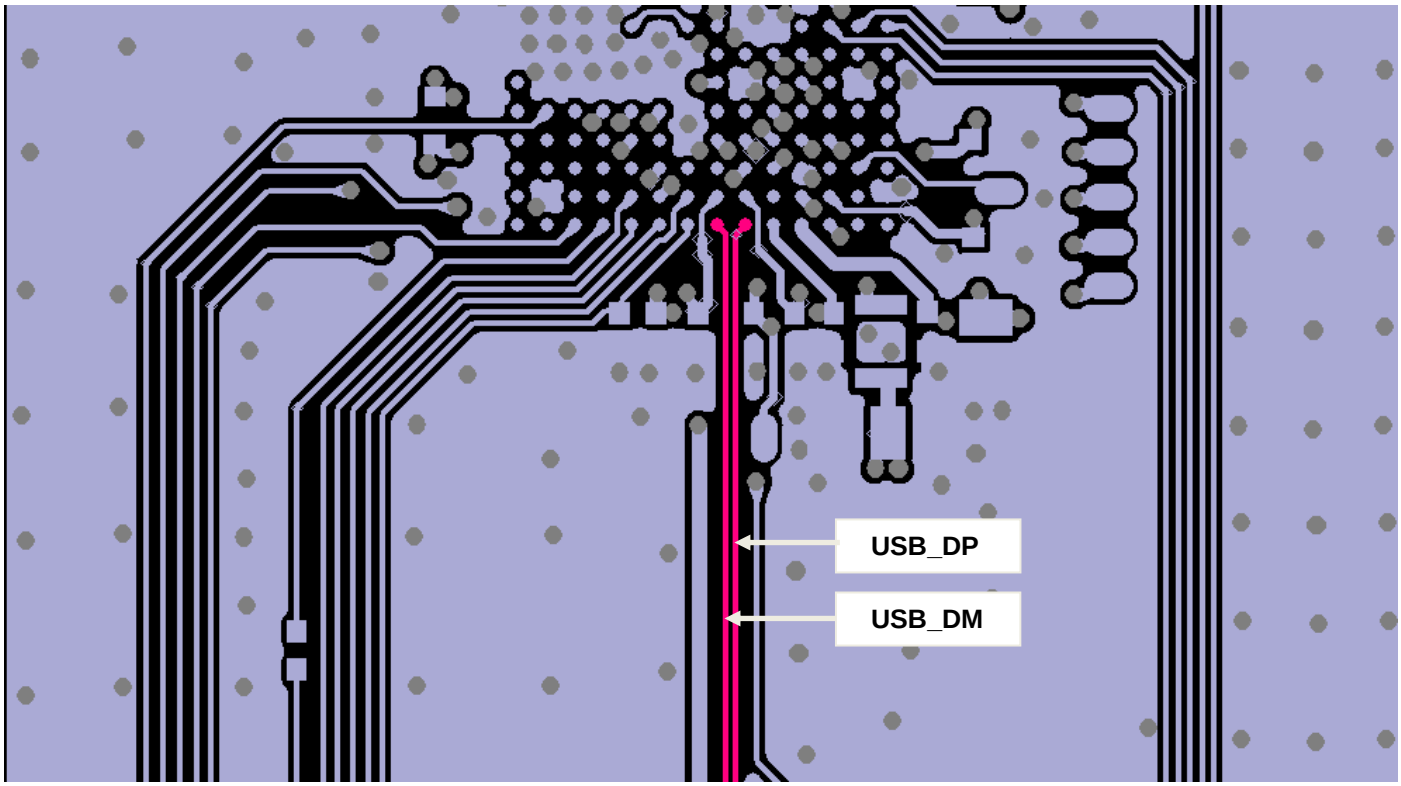

Figure 5: USB Signals Routing in Layer 1

6 UART Layout Guidelines

The following guidelines must be followed for UART signals. The signals are UART1_TX, UART1_RX, UART1_RTS, UART1_CTS.

1. Keep the UART signals away from noisy sources or other sensitive signals.
2. UART signals can be routed with multiple vias. However, ensure return path is closer to the signals.

The image below shows UART traces routing in Layer 1, as an example.

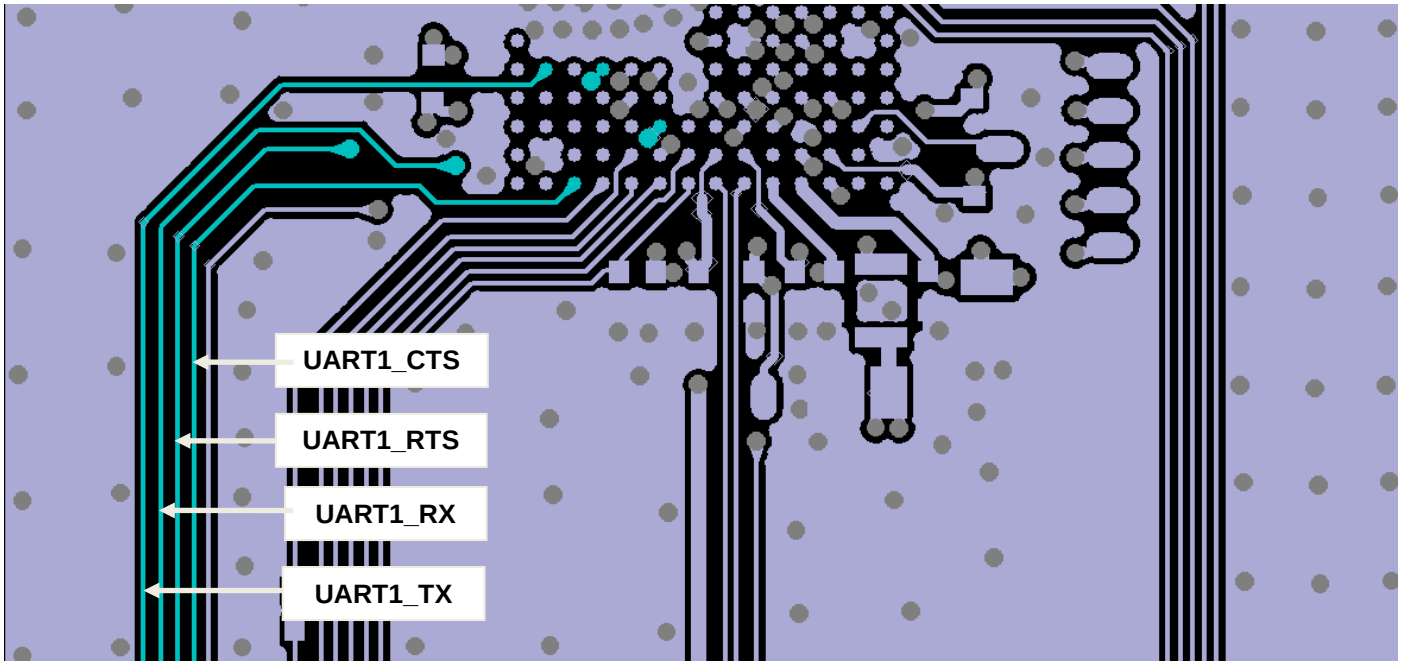

Figure 6: UART Signals Routing in Layer 1

UART1_RX and UART1_RTS pins are located inside. So, traces for these two signals can be routed in Layer 4 as shown below.

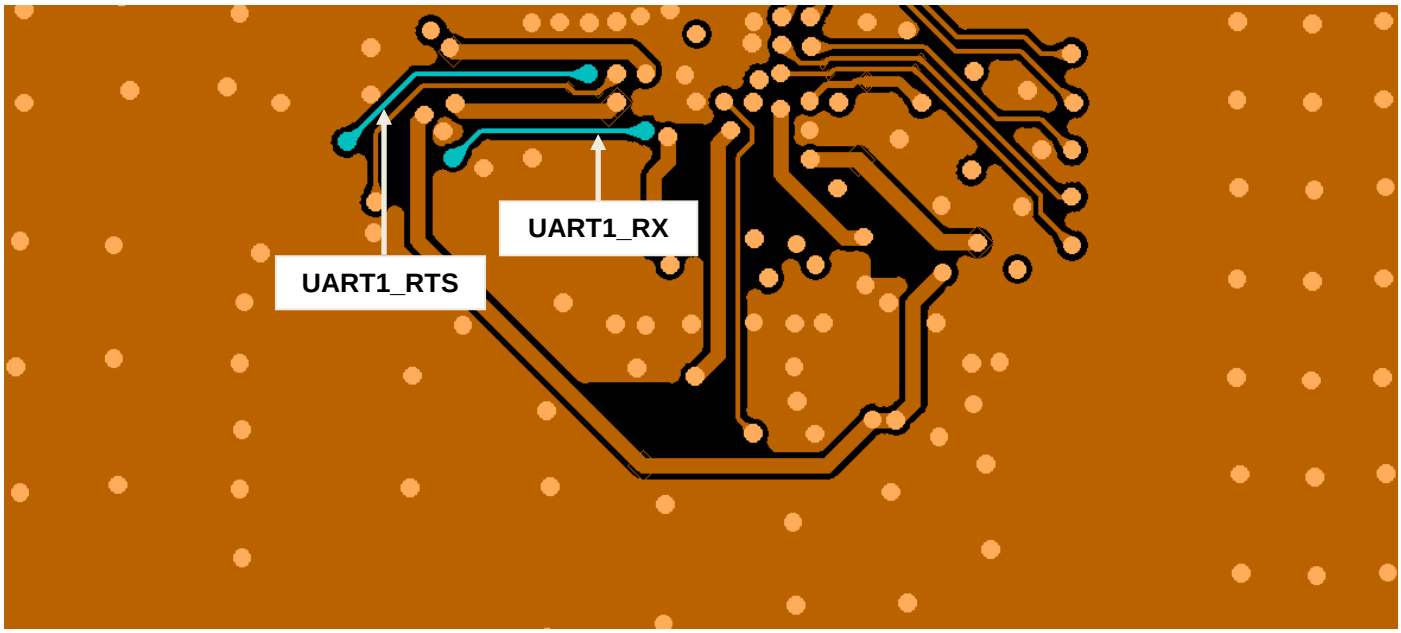

Figure 7: UART Signals Routing in Layer 4

7 Power Supply Layout Guidelines

There are many power pins on the CC0 module. Careful routing with appropriate trace widths must be followed for better power delivery to the module. Follow the guidelines below for all the power traces.

1. The following power supply pins needs to be STAR routed from the Supply Source.
    a. VINBCKDC
    b. ULP_IO_VDD
    c. SDIO_IO_VDD
    d. IO_VDD_1
    e. UULP_VBATT_1
    f. UULP_VBATT_2
    g. PA2G_AVDD
    h. PA5G_AVDD
    i. RF_VBATT
    j. RF_AVDD33
    k. AVDD_1P9_3P3

2. The layout guidelines for the BUCK circuitry are as follows.

    Minimize the loop area formed by inductor switching node, output capacitors, and input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance and resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components.
    a. VINBCKDC Capacitor should be very close to the Chip Pin and the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    b. Buck Inductor should be close to Chip VOUTBCKDC pin and buck capacitor should be placed closer to the Inductor. The Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    c. The Ground Plane underneath the Buck Inductor in Layer 1 should be made as an isolated copper patch and should descend to the Second Layer (main Ground plane) through multiple Vias.
    d. The path from VOUTBCKDC to VINLDOSOC is a high current path. The Trace should be as short and wide as possible and is recommended to run Grounded Shield Traces on either side of this High Current Trace.
    e. The Capacitor on VINLDOSOC should be very close to the Chip Pin, and the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
3. If any power supply trace or shape needs to change layers from a layer referencing (adjacent to) the top ground plane to the bottom ground plane in the stack-up or vice versa, an equal number of ground vias should be interspersed with, or placed immediately adjacent to the vias carrying the supply voltage. This minimizes noise coupling from the supply to nearby signals and other supplies.
4. The width of power traces must be a minimum of 15 mils. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
5. Place decoupling capacitors near target power pins. If possible, keep them on the same side as the module, to avoid inductance due to vias.

The image below shows example layout of Internal Buck regulator's Power Supply traces routing in Layer 1.

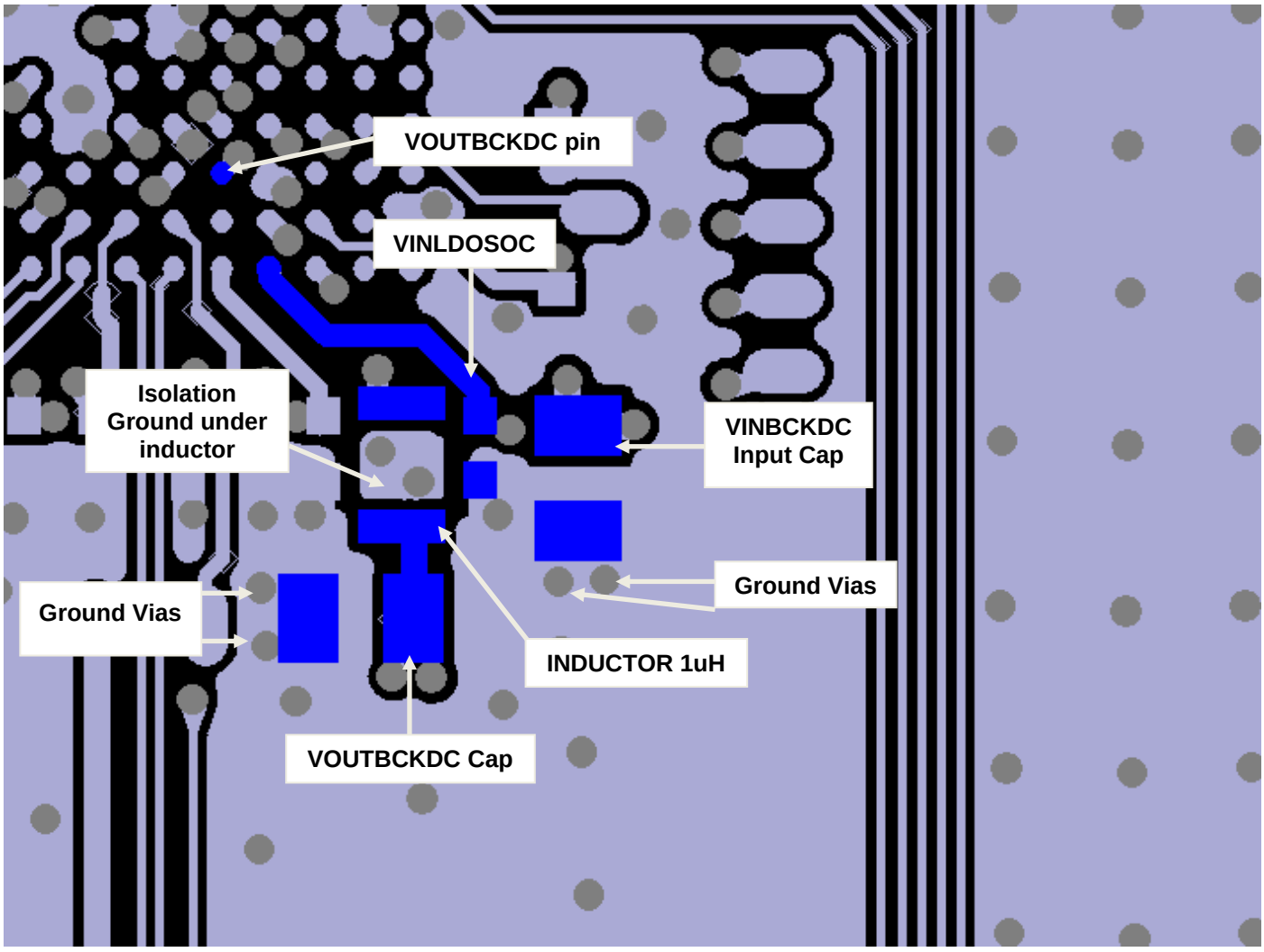

Figure 8: Internal Buck Regulator Circuitry Routing in Layer 1

The image below shows some of the Power Supply traces routing in Layer 3. As shown, they are routed in Star fashion from the supply source.

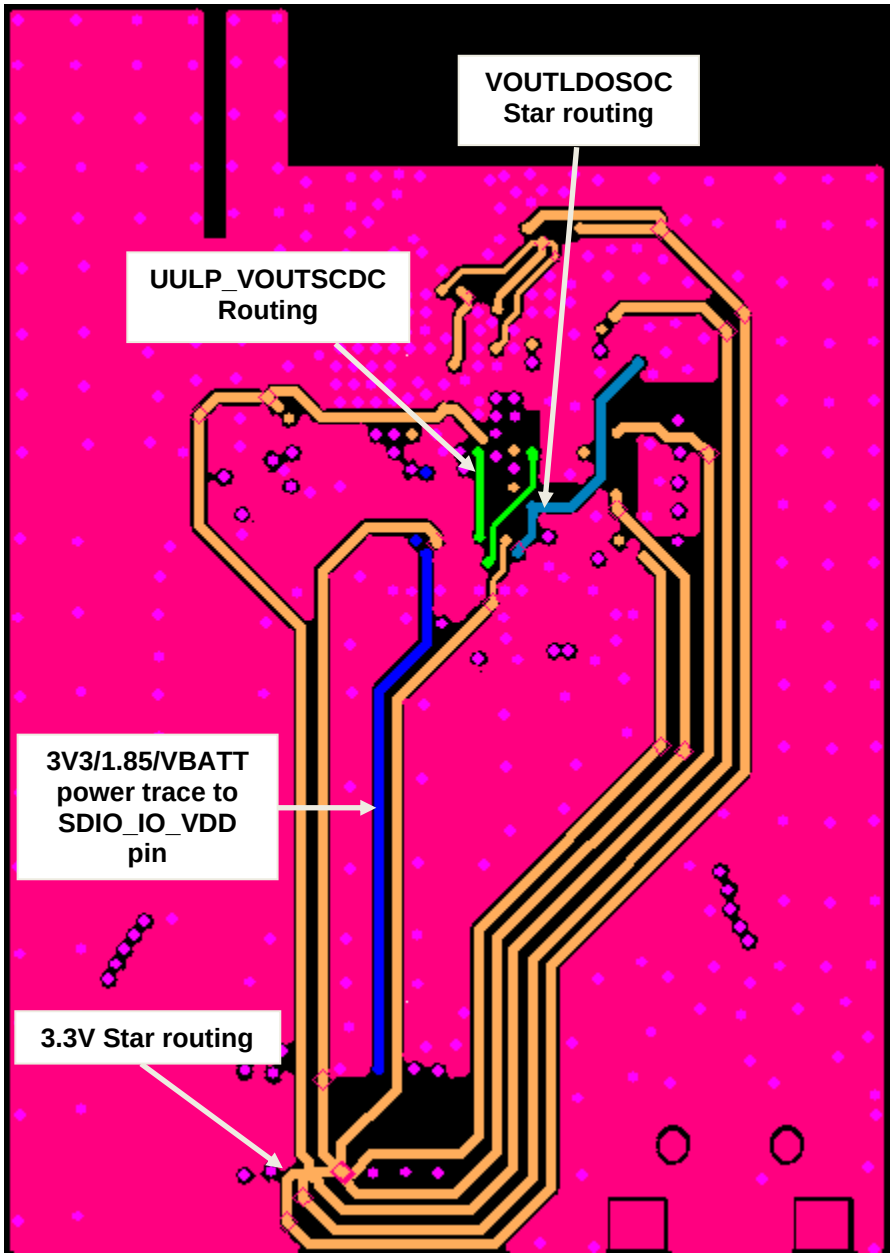

Figure 9: Power Supply Routing in Layer 3

The image below shows Power Supply traces routing in the Layer 4. As shown, they are routed in Star fashion from the supply source.

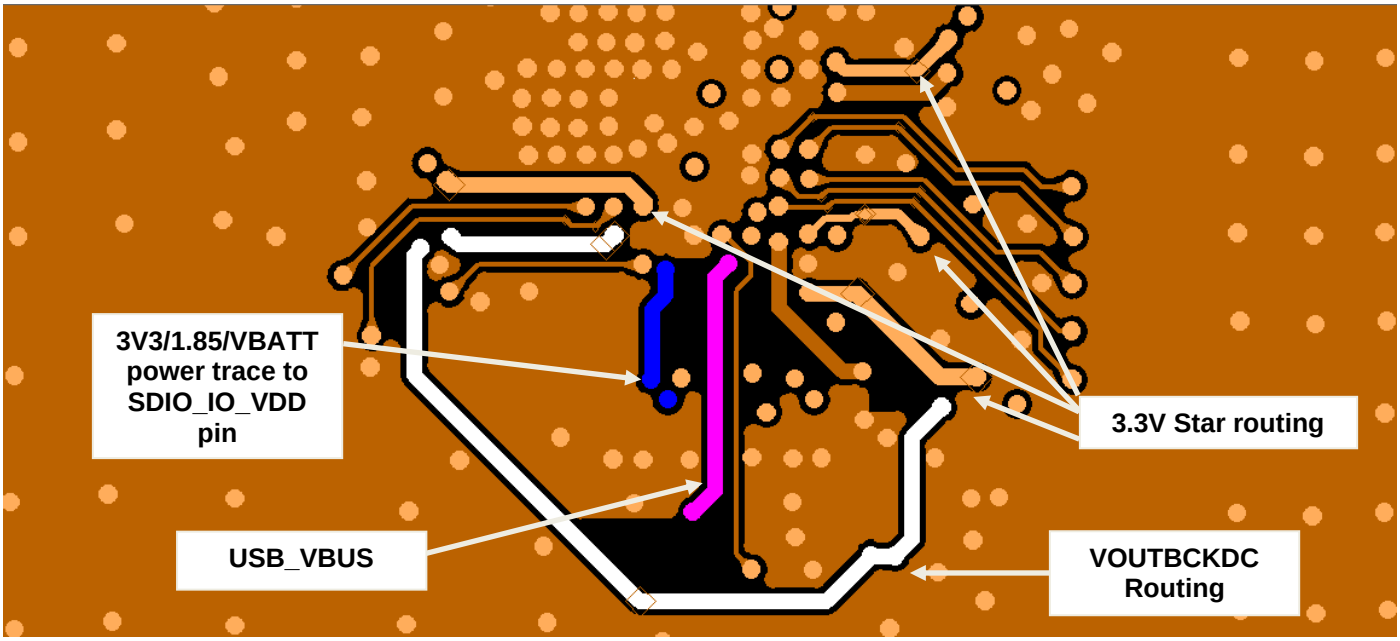

Figure 10: Power Supply Routing in Layer 4

8 GND Layout Guidelines

All the returns paths of critical signals like RF, high speed signals like SPI/SDIO/USB and Power, flow through GND. So, GND carries lot of return currents and high speed signals. Designer must ensure return paths are short. There are various possible ways to achieve good grounding, and below guidelines provide some of the possible insights into it.

1. Dedicate the adjacent layer of the CC0 module and its circuitry to GND. In this Application Note, the CC0 module and the circuitry are placed in Layer 1, so Layer 2 must be completely GND plane only.
2. GND pour must be continuous with no voids.
3. Pour GND in all the empty spaces around parts and traces in all the layers. Stitch this GND pour to GND plane using multiple GND vias.
4. Avoid large GND fill without GND vias. Else it acts like an antenna, and this can possibly cause radiation of unwanted signals affecting other parts of the board. This can negatively affect board performance.

Below image shows complete GND plane in Layer 2. Also, you can observe from images in above sections, that all the empty spaces are filled with GND pour and stitched with GND vias to the GND plane.

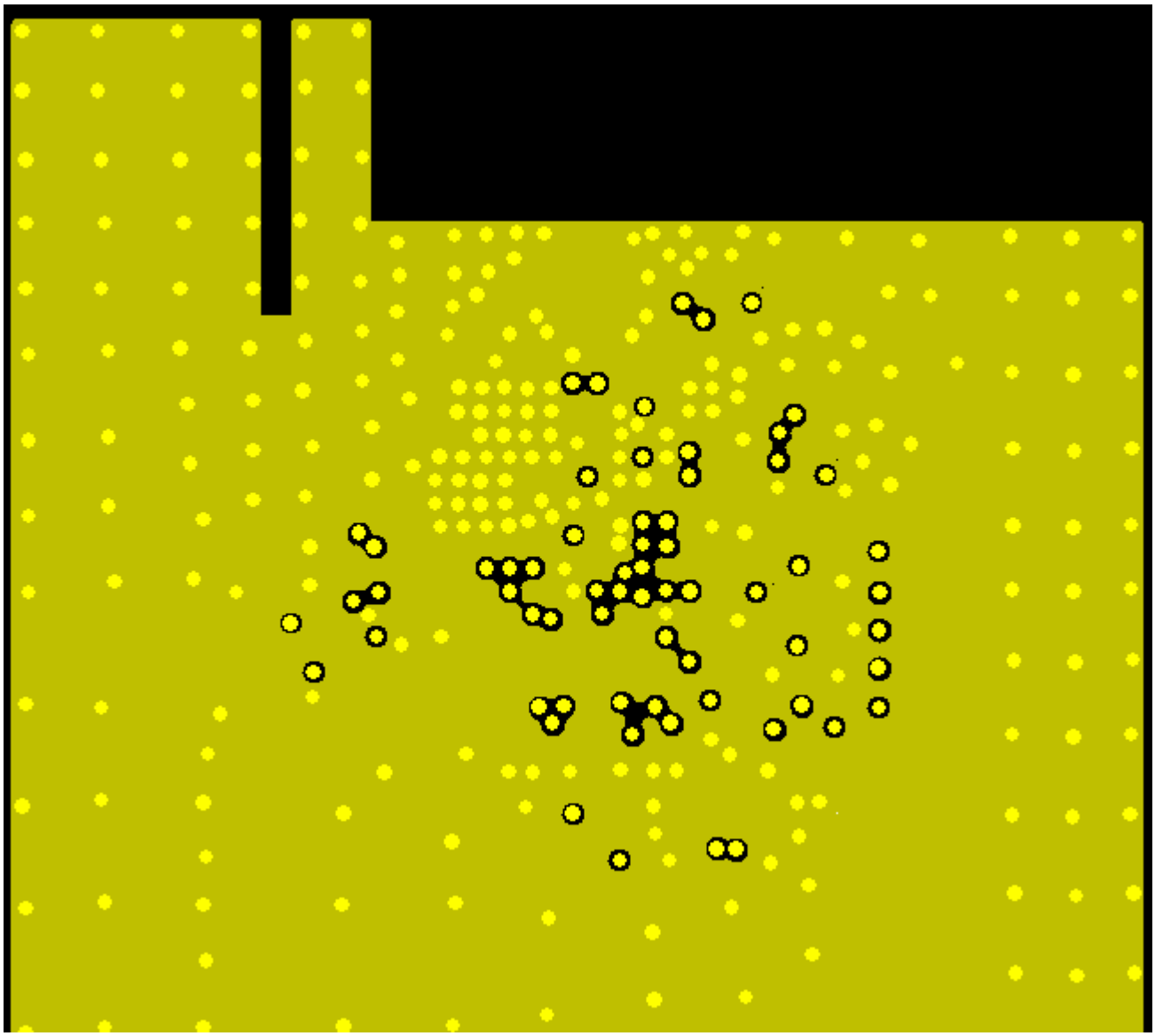

Figure 11: GND Plane in Layer 2

The image below shows the example picture of GND pour in Layer 1 with one just via. Such hanging GND pour must be avoided. Stitch GND vias near the periphery of the GND pour, or else restrict such GND pour shapes.

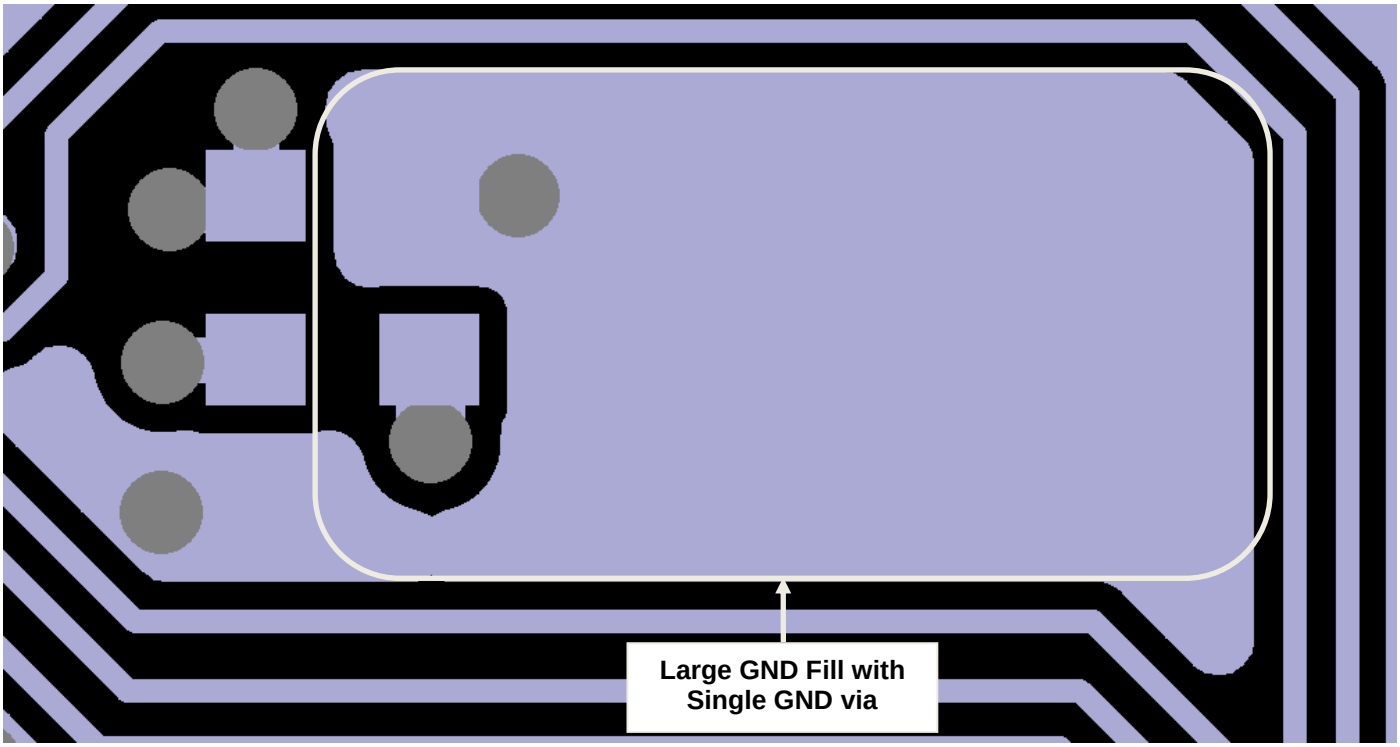

Figure 12: Hanging GND Pour

9 Revision History

Revision No	Version No	Date	Changes
1	1.0	Jun, 2021	Initial version
2	1.1	Aug, 2021	Added Figures titles and numbers

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