AN1342: RS9116 CC1 Board Layout Guidelines

Version 1.1

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Table of Contents

1 Introduction

This Application Note provides PCB layout guidelines for the RS9116 CC1 module. These guidelines cover parts placement, various critical traces routing like RF, Host interfaces routing like SDIO/SPI, USB, UART, power routing, and GND pour. CC1 module placement and routing can be done within 4-layer PCB stack-up. However, designers can choose higher number of layers, based on product needs. This document describes placement and routing considering a 4-layer stack-up setup.

Below is the recommended layer stack-up and placement/routing considering a 4-layer stack-up. Exact PCB thickness can be as per the layer stack-up provided by the PCB manufacturer. It is recommended to use a PCB thickness close to 1.6 mm, but designers can choose suitable thickness based on product needs.

- Layer 1 : Parts Placement, Interface signals (SDIO/SPI, USB, UART)
- Layer 2 : GND
- Layer 3 : Power supply star routing
- Layer 4 : Power supply star routing, USB & UART Interface signals and GPIOs

2 Placement Guidelines

Here are the recommendations for the placement of the CC1 module and its associated parts. Parts are placed on the same side of the CC1 module, in this Application Note. However, designers can choose to place them on either side of PCB for achieving best placement and routing. Designers can use suitable antenna as per the product needs, like on-board PCB trace, External PCB trace, Dipole, etc. The following steps can be sequentially followed to achieve optimal placement.

1. To get the best RF performance from CC1 circuitry and antenna, it is recommended to place the module near the PCB edge. Antenna part guidelines must be followed for its placement and routing.
2. Decoupling capacitors are recommended to be placed on intended power pins. Decaps must be placed within 5 mm distance from the module pins.
3. VIN_3P3 Capacitor should be placed within 10mm distance from the module pin.
4. Series resistor on Clock signal of SPI or SDIO interface, must be placed close to the source of this clock signal. It must not be placed near the module end of the signal.

Considering the above recommendations, the CC1 module and its circuitry can be placed on single side of PCB as shown below. This takes 20 mm x 20 mm of board space approximately. Designers can choose to place the components different from the below recommendation to suit the product needs.

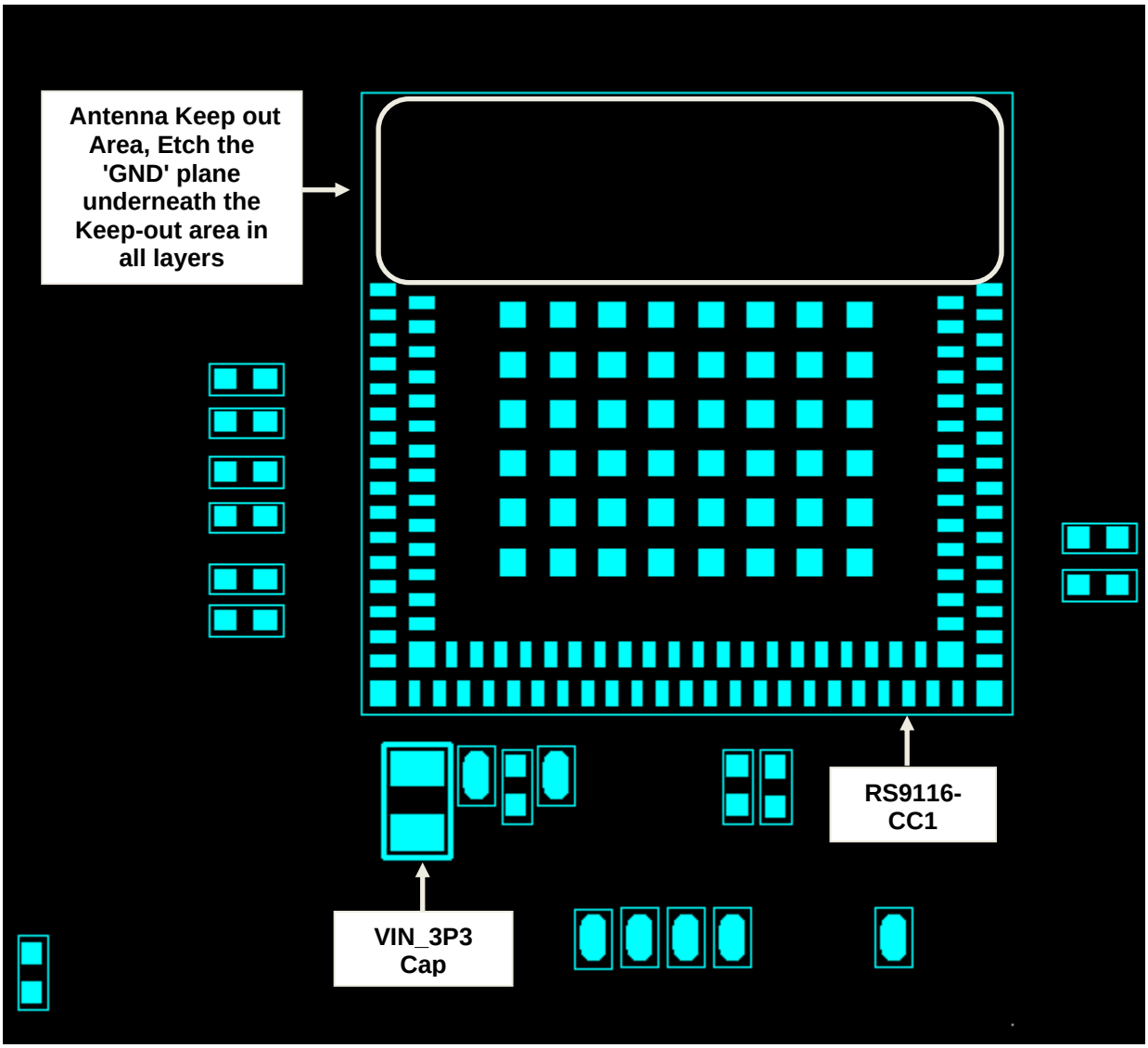

Figure 1: CC1 Module and Components Placement

3 Antenna Layout Guidelines

The CC1 module has an integrated PCB trace antenna, and it works at both 2.4 GHz and 5 GHz. This antenna must be positioned toward outer periphery of the PCB edge. There is also a U.FL connector on the module, through which an external antenna can be connected. The choice between the on-board antenna and the external antenna can be made through a software command. The guidelines below must be followed to get best RF performance from the PCB antenna and antenna connected to U.FL connector.

1. There should be no metal planes or traces in the region under the PCB antenna and beside it for at least 3 mm. The module should be placed such that the antenna portion is on the edge of the PCB. The figure below may be used as a reference.

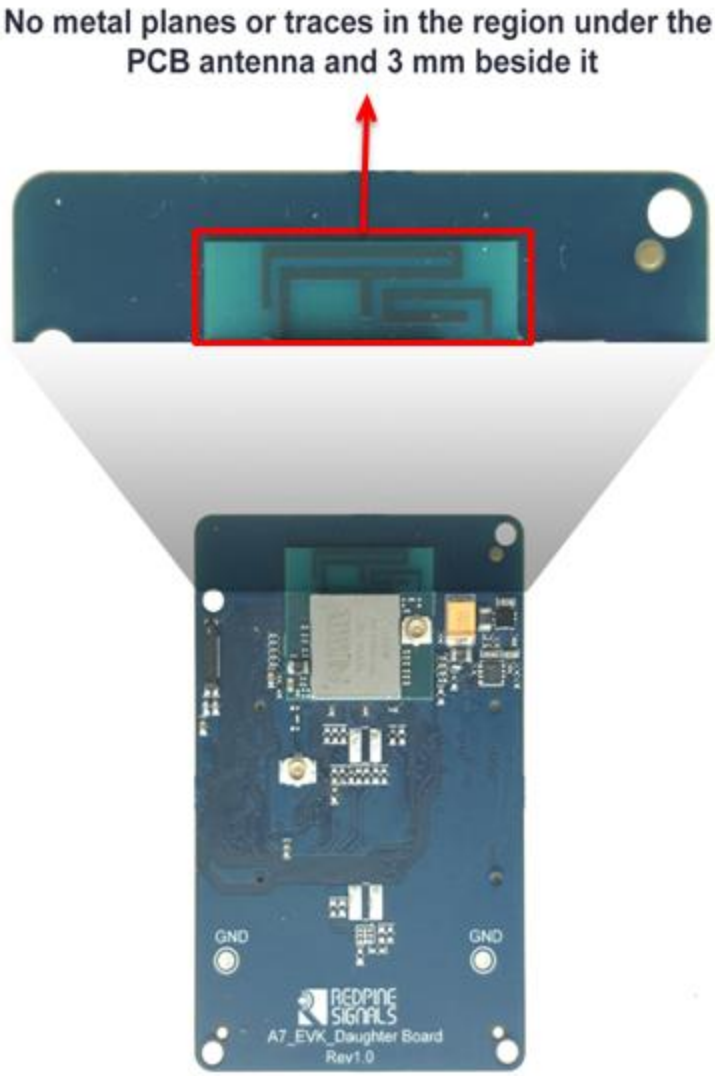

Figure 2: PCB Antenna Layout Requirement

2. The figures below show the U.FL connector integrated on the module and mating connector with external antenna. The connector on the external antenna should be pushed down to fit into the U.FL connector connected to the module.

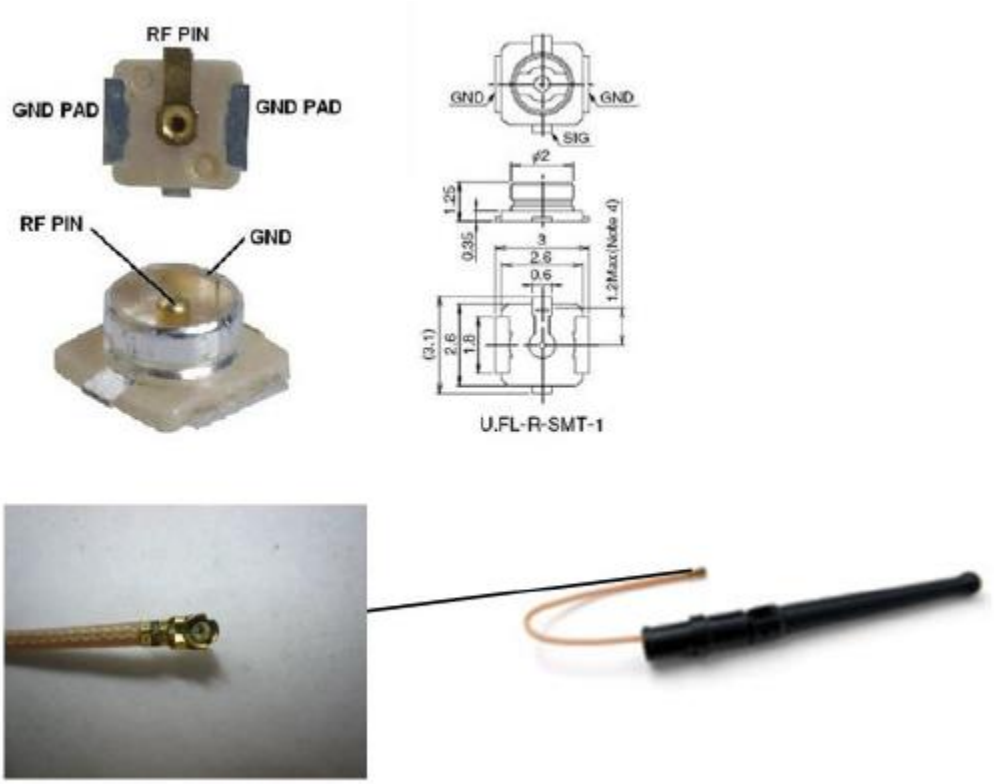

Figure 3: U.FL Connector Details

4 SDIO/SPI Layout Guidelines

SDIO and SPI are high speed interfaces where-in clock signals can reach up to 100 MHz. High speed design guidelines like below must be followed for the signals in these interfaces. SDIO/SPI signals include SDIO_CLK/SPI_CLK, SDIO_CMD/SPI_CSN, SDIO_D0/SPI_MOSI, SDIO_D1/SPI_MISO, SDIO_D2/SPI_INTR, SDIO_D3.

1. The characteristic impedance of the SDIO/SPI lines should be 50 Ω.
2. Match the lengths of all SDIO/SPI lines within 100 mils tolerance.
3. Keep the SDIO_CLK/SPI_CLK trace away from nearby traces with minimum 2x distance.
4. Do not route any parallel traces above or underneath the SDIO_CLK/SPI_CLK trace.
5. Keep SDIO/SPI traces away from all clock lines and noisy power supply components such as the switcher inductors. Avoid crossing over power supplies or ground discontinuities. SDIO/SPI traces must have a solid ground on the layer adjacent to them.
6. Do not leave any stubs on the SDIO/SPI traces.

The image below shows the SDIO/SPI traces routing in Layer 1, as an example. The series resistor on SDIO_CLK/SPI_CLK is placed closer to the source of this clock, rather than placing closer to the CC1 module.

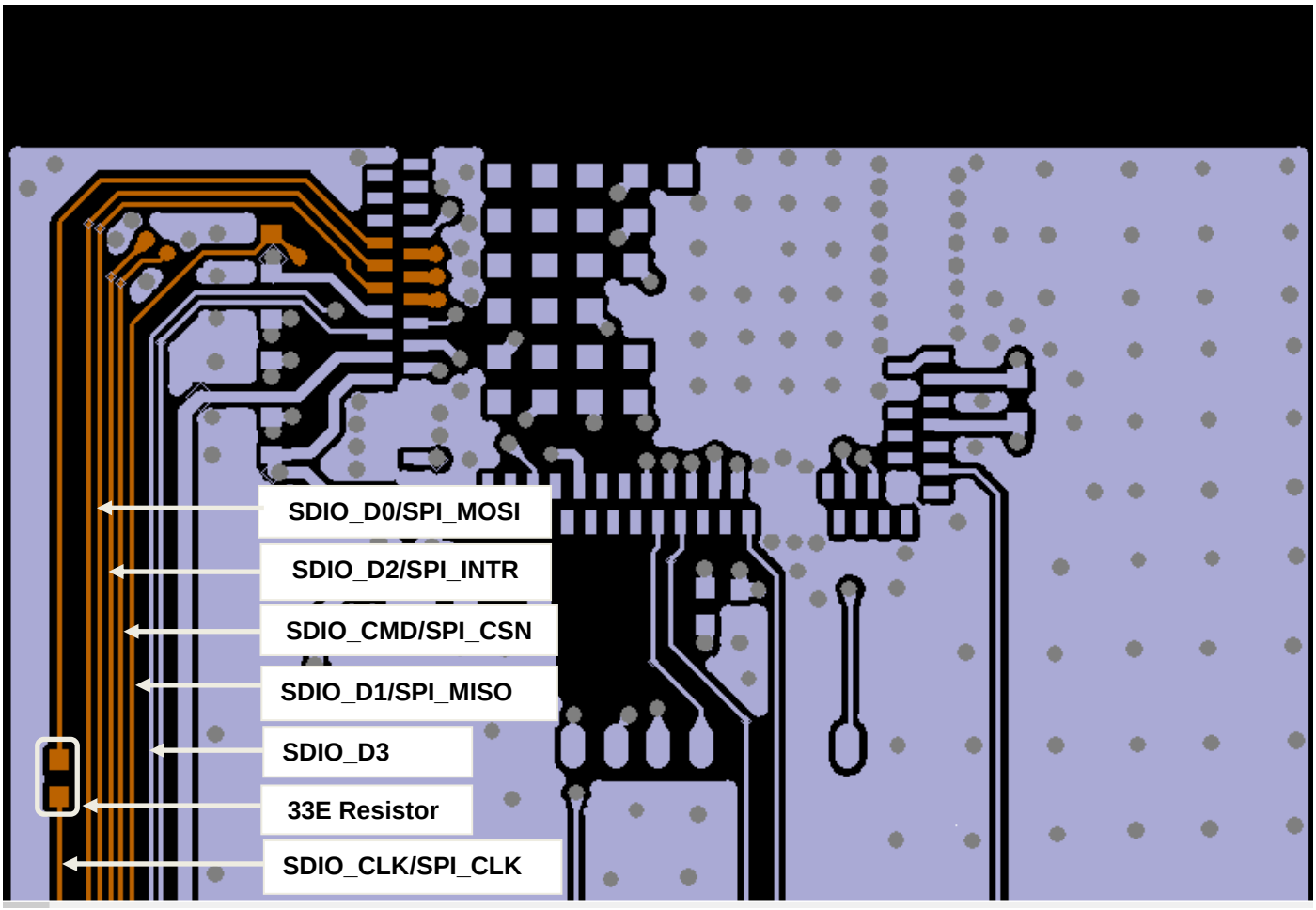

Figure 4: SDIO/SPI Signals Routing in Layer 1

Since SDIO_CMD/SPI_CSN, SDIO_D1/SPI_MISO, SDIO_D3 signals are present on the inner row pins of the module, these must be routed in Layer 4 as shown below.

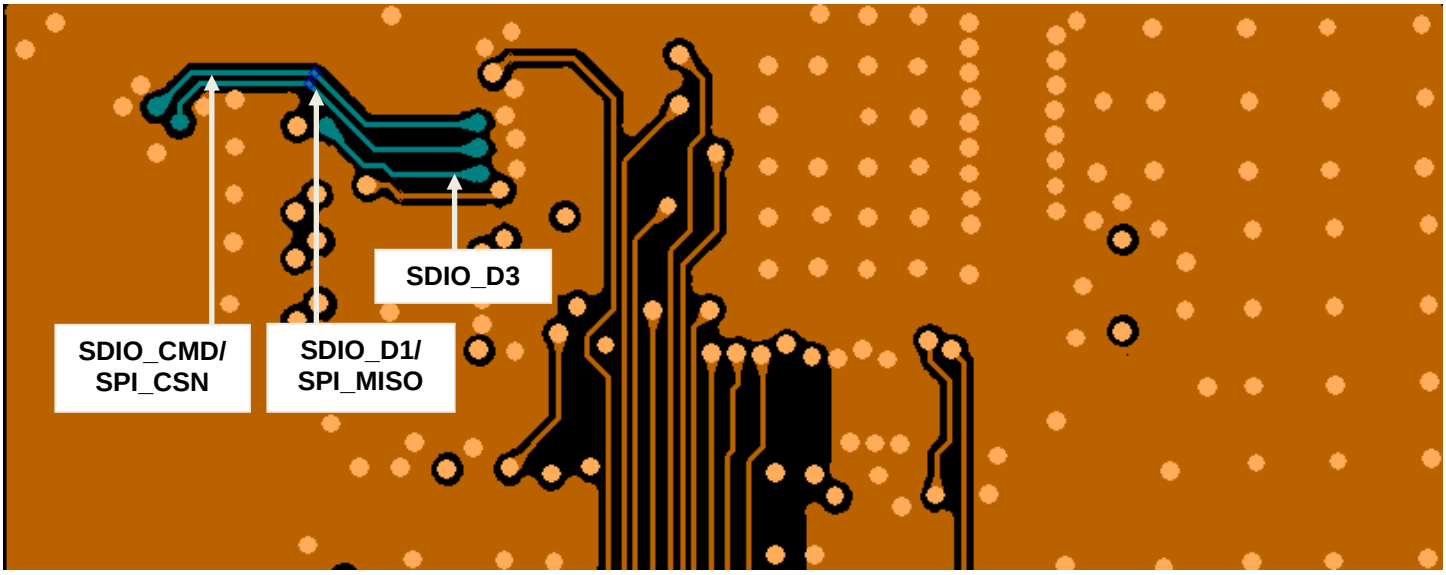

Figure 5: SDIO/SPI Signals Routing in Layer 4

5 USB Layout Guidelines

USB signals can reach speeds of 480 Mbps. Guidelines for the differential signals USB_DP and USB_DM must be followed.

1. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (i.e., a) that achieves 90 Ω of differential impedances and 45 Ω for each trace.
2. To minimize crosstalk between the two USB differential signals (USB_DP and USB_DN) and other signal traces routed close to them, it is recommended that a minimum spacing of 3xa be maintained for low-speed non-periodic signals and a minimum spacing of 7xa be maintained for high-speed periodic signals.
3. It is recommended that the total trace length of the signals between RS9116 part and USB connector (or USB host part) be less than 450 mm.
4. If the USB high-speed signals are routed on the Top layer, best results will be achieved if Layer 2 is a continuous GND plane. Furthermore, there must be only one ground plane under high-speed signals and avoid the high-speed signals crossing from GND plane to another GND plane.
5. Do not route the USB differential lines close to edge of the board.

The image below shows USB differential traces routing in Layer 1, as an example.

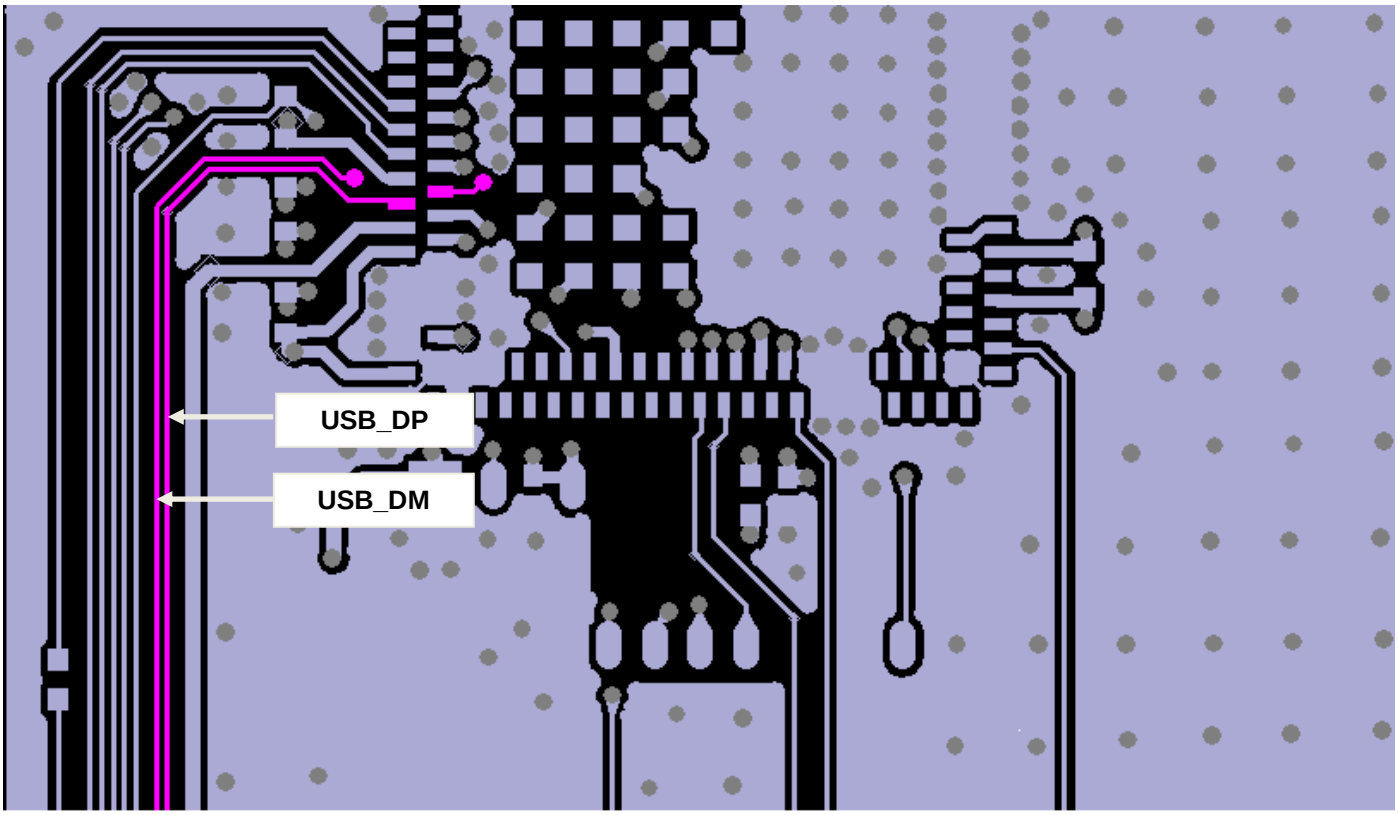

Figure 6: USB Signals Routing in Layer 1

6 UART Layout Guidelines

The guidelines below must be followed for UART signals. The signals are UART1_TX, UART1_RX, UART1_RTS, UART1_CTS.

1. Keep the UART signals away from noisy sources or other sensitive signals.
2. UART signals can be routed with multiple vias. However, ensure return path is closer to the signals.

The image below shows UART traces routing in Layer 1, as an example.

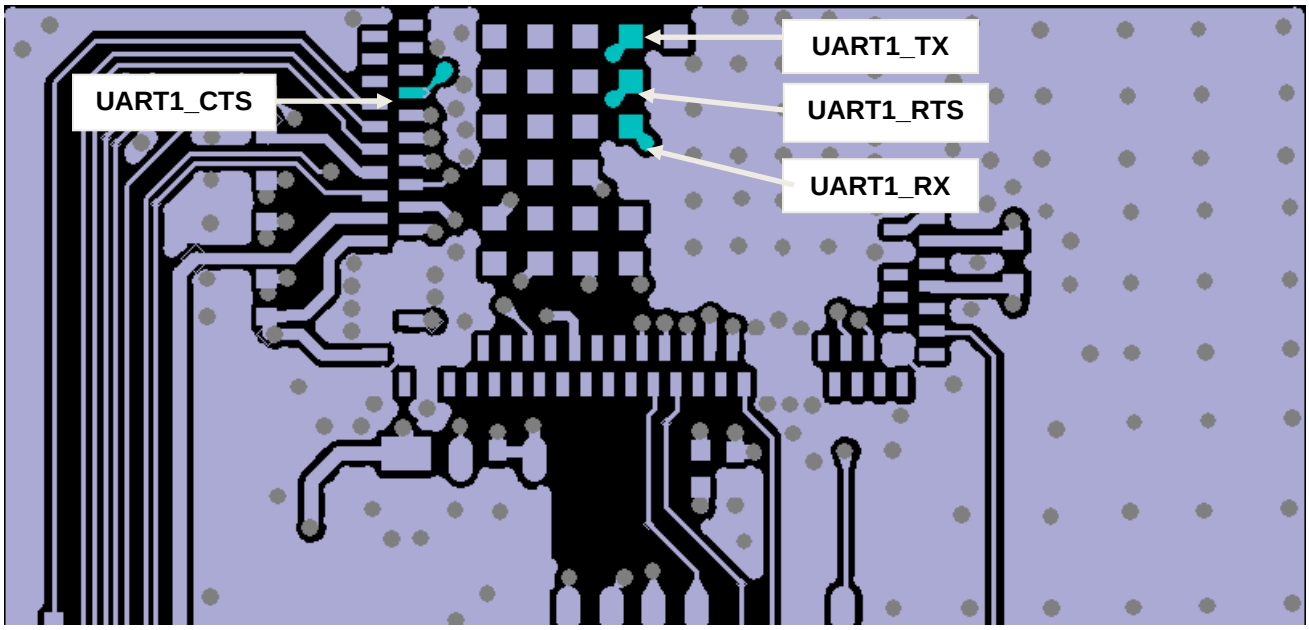

Figure 7: UART Signals Routing in Layer 1

All the UART pins are located inside. So, traces for these signals can be routed in Layer4 as shown below.

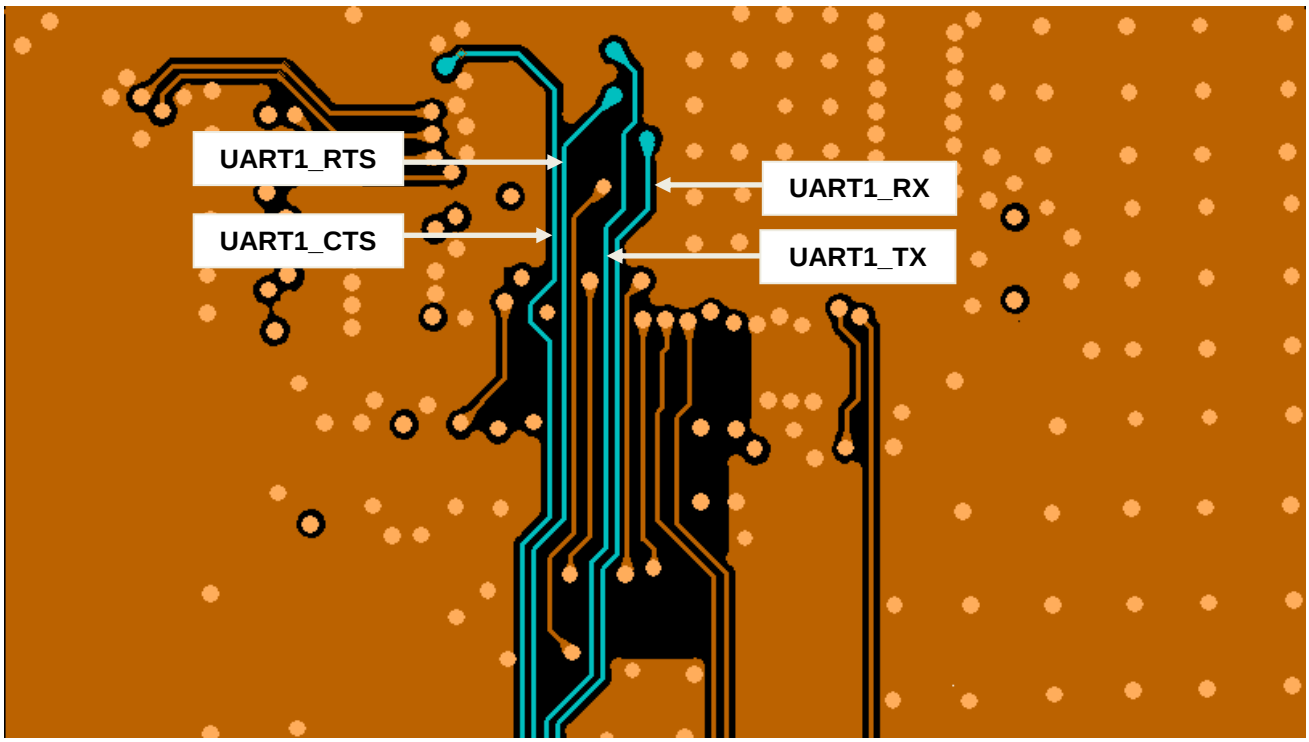

Figure 8: UART Signals Routing in Layer 4

7 Power Supply Layout Guidelines

There are many power pins on the CC1 module. Careful routing with appropriate trace widths must be followed for better power delivery to the module. Follow the guidelines below for all the power traces.

1. The following power supply pins needs to be STAR routed from the Supply Source.
    a. VIN_3P3
    b. UULP_VBATT_1
    c. PA5G_AVDD
    d. ULP_IO_VDD
    e. SDIO_IO_VDD
    f. AVDD_1P9_3V3
    g. RF_AVDD33

2. If any power supply trace or shape needs to change layers from a layer referencing (adjacent to) the top ground plane to the bottom ground plane in the stack-up or vice versa, an equal number of ground vias should be interspersed with, or placed immediately adjacent to the vias carrying the supply voltage. This minimizes noise coupling from the supply to nearby signals and other supplies.
3. The width of power traces must be a minimum of 15 mils. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
4. Place decoupling capacitors near target power pins. If possible, keep them on the same side as the module, to avoid inductance due to vias.

The image below shows example layout of VIN_3P3, VOUTLDOSOC and USB_VBUS Power Supply traces routing in Layer 1.

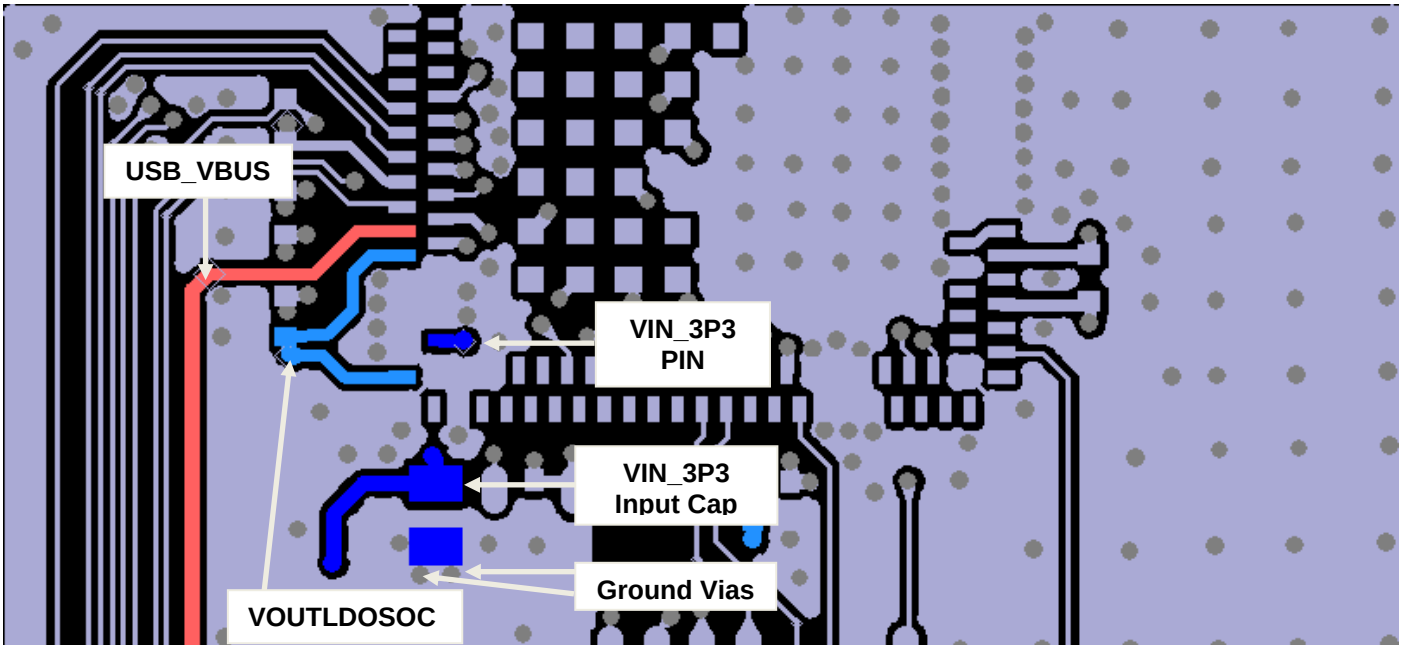

Figure 9: Power Supply Routing in Layer 1

The image below shows some of the Power Supply traces routing in Layer 3. As shown, they are routed in Star fashion from the supply source.

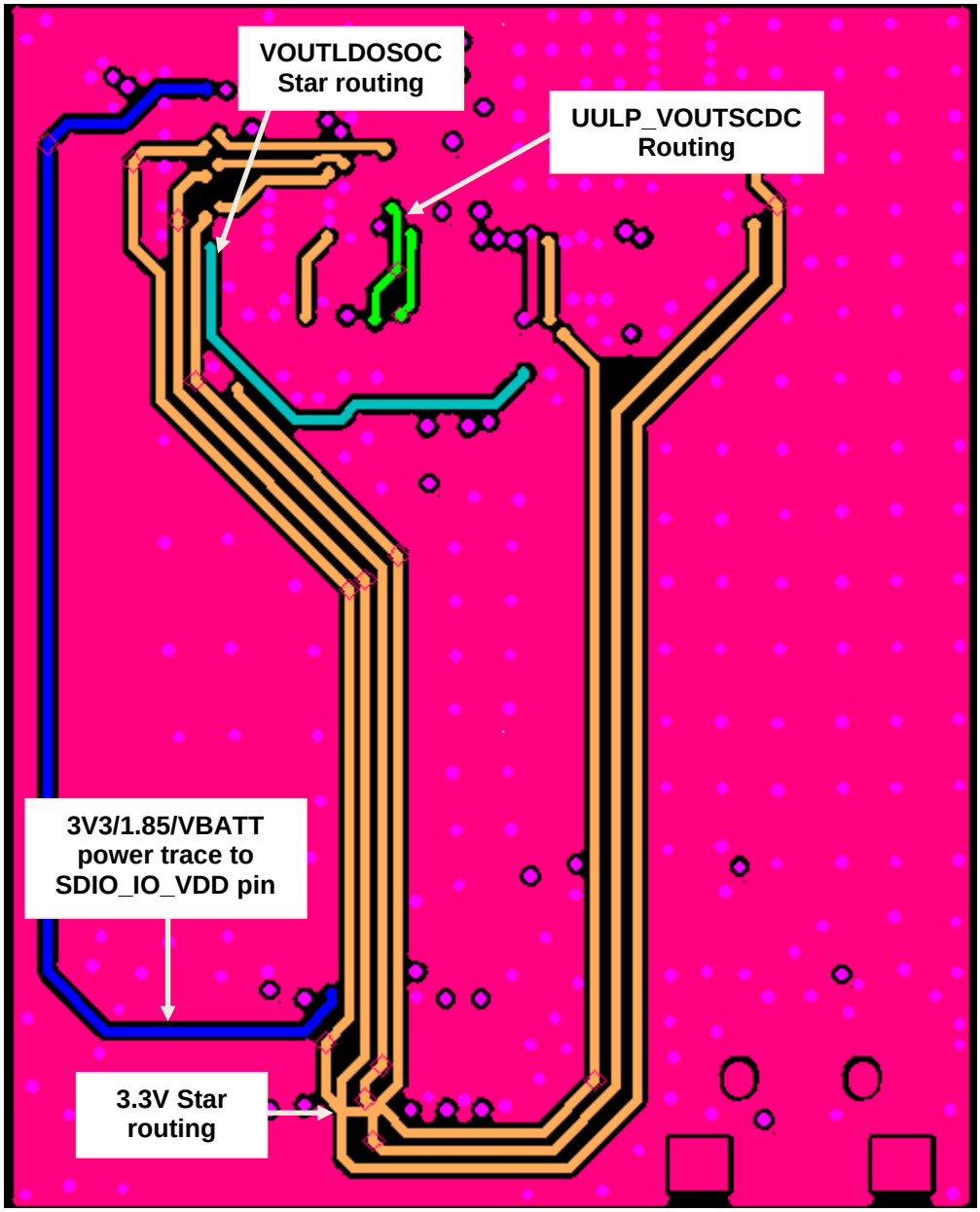

Figure 10: Power Supply Routing in Layer 3

8 GND Layout Guidelines

All the returns paths of critical signals like RF, high speed signals like SPI/SDIO/USB and Power, flow through GND. So, GND carries lot of return currents and high speed signals. Designer must ensure return paths are short. There are various possible ways to achieve good grounding, and below guidelines provide some of the possible insights into it.

1. Dedicate the adjacent layer of the CC1 module and its circuitry, to GND. In this Application Note, the CC1 module and the circuitry are placed in Layer 1, so Layer 2 must be completely GND plane only.
2. GND pour must be continuous with no voids.
3. Pour GND in all the empty spaces around parts and traces in all the layers. Stitch this GND pour to GND plane using multiple GND vias.
4. Avoid large GND fill without GND vias. Else it acts like an antenna, and this can possibly cause radiation of unwanted signals affecting other parts of the board. This can negatively affect board performance.

The image below shows the complete GND plane in Layer 2. Also, the images in the sections above show that all the empty spaces are filled with GND pour and stitched with GND vias to the GND plane.

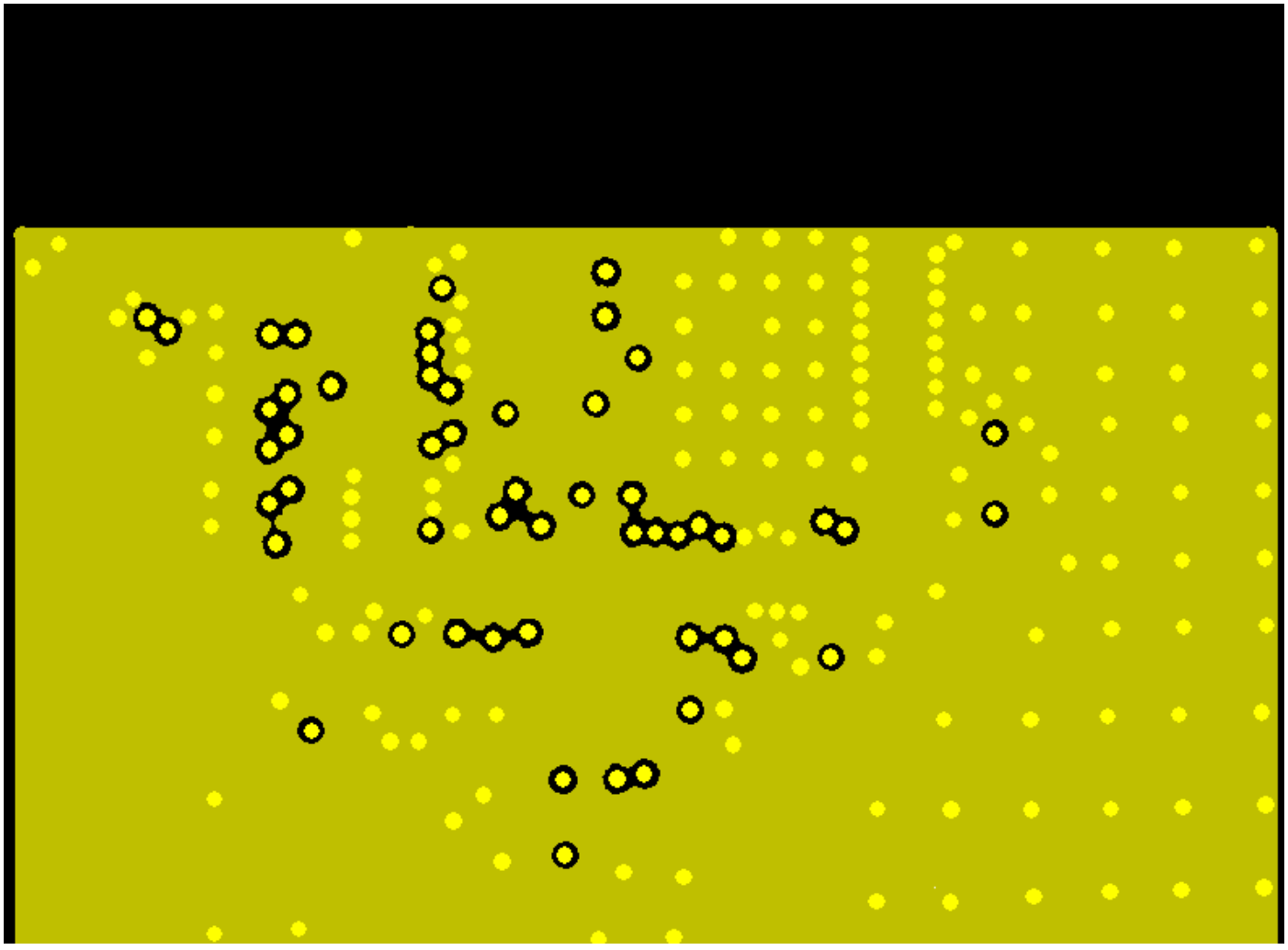

Figure 11: GND Plane in Layer 2

The following image shows the example picture of GND pour in Layer 1 with one just via. Such hanging GND pour must be avoided. Stitch GND vias near the periphery of the GND pour, or else restrict such GND pour shapes.

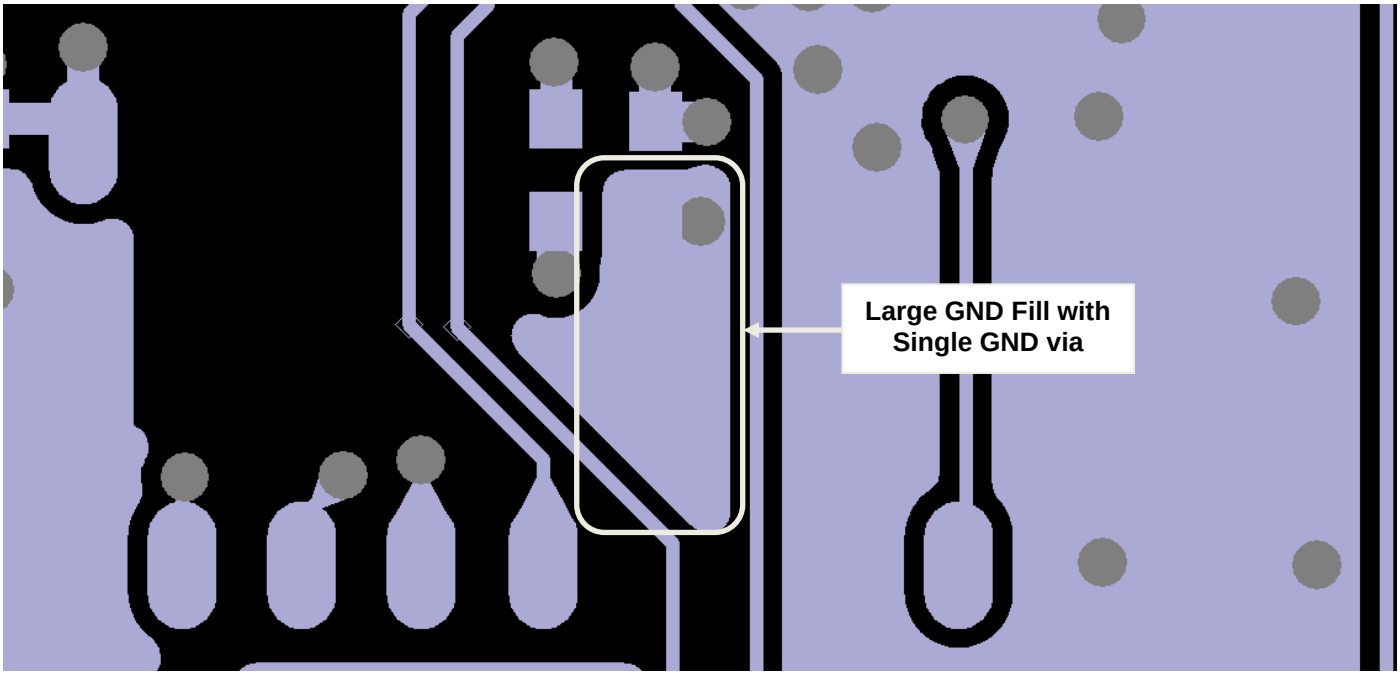

Figure 12: Hanging GND Pour

9 Revision History

Revision No	Version No	Date	Changes
1	1.0	Jun, 2021	Initial version
2	1.1	Aug, 2021	Added Figures titles and numbers

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