AN1344: RS9116 QMS Board Layout Guidelines

Version 1.0

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1 Introduction

This Application Note provides PCB layout guidelines for designing a PCB using the RS9116 QMS SoC. These guidelines cover parts placement, routing of various critical traces like RF, host interfaces routing like SDIO/SPI, USB, UART, power routing, and GND pour. QMS SoC placement and routing can be done within a 4-layer PCB stack-up. However, the designer can choose a higher number of layers, based on product needs. This Application Note describes placement and routing considering a 4-layer stack-up.

The recommended layer stack-up and placement/routing considering a 4-layer stack-up is listed below. The exact PCB thickness can be according to the layer stack-up provided by the PCB manufacturer. It is recommended to use a PCB thickness close to 1.6 mm, but the designer can choose a suitable thickness based on product needs.

- Layer 1 : Parts Placement, RF circuitry, Interface signals (SDIO/SPI, USB, UART), Crystal
- Layer 2 : GND
- Layer 3 : Power supply star routing
- Layer 4 : Power supply star routing and few GPIOs

2 Placement Guidelines

The designer can choose a suitable antenna as per the product needs, like a chip antenna, on-board PCB trace, external PCB trace, dipole, etc. The design described in this Application Note uses a chip antenna.

Here are the recommendations for the placement of QMS SoC and its associated parts. Parts are placed on the same side as the QMS SoC in this document. However, the designer can choose to place them on either side of PCB for achieving best placement and routing. The steps below can be sequentially followed to achieve optimal placement.

1. To get the best RF performance from QMS SoC and antenna, it is recommended to place antenna circuitry near the PCB edge. Antenna part guidelines must be followed for its placement and routing.
2. Place RF components, antenna and QMS SoC on the same side of PCB, so that there are no vias on RF traces.
3. RF front-end components and QMS SoC should be placed at minimal distance from RF ports (on QMS) to the antenna, so that RF traces lengths are as short as possible.
4. Decoupling capacitors are recommended to be placed on the intended power pins. Decaps must be placed within 5 mm distance from the module pins.
5. VINBCKDC capacitor should be placed within 10 mm distance from the module pin.
6. Buck inductor should be placed within 5 mm distance from VOUTBCKDC pin. Buck capacitor should be placed within 1 mm distance from the Buck inductor.
7. The series resistor on Clock signal of SPI or SDIO interface must be placed close to the source of this clock signal. It must not be placed near the module end of the signal.

Considering the above recommendations, the QMS SoC and its circuitry can be placed on a single side of the PCB as shown below. This takes less than 25 mm x 20 mm of board space approximately, until RF antenna tuning network. The designer can choose to place the components better than what is shown below to suit the product needs.

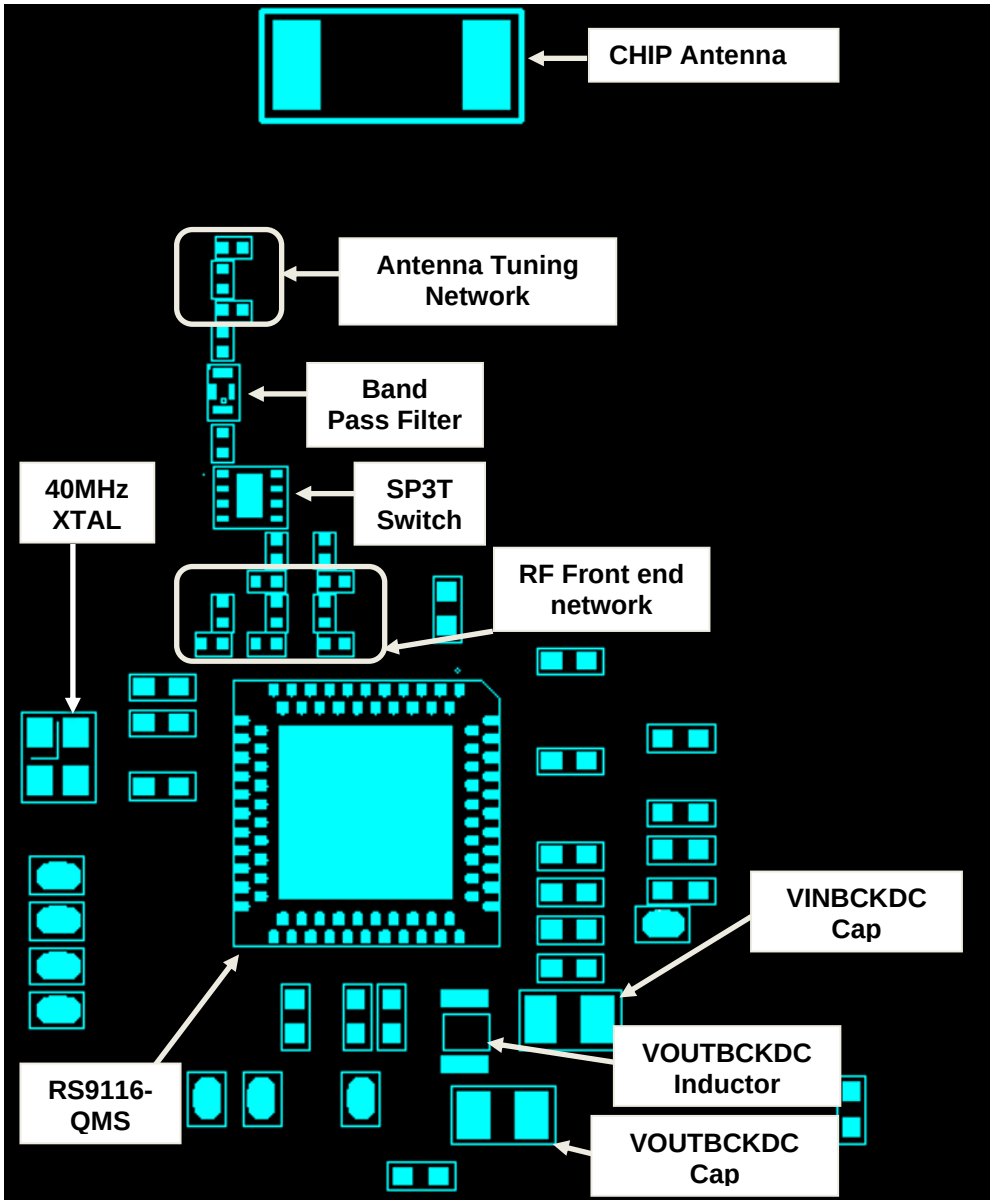

Figure 1: QMS SoC and Components Placement

3 RF Layout Guidelines

RF parts placement and trace routing affect the RF performance of the SoC and circuitry. Great care must be taken to ensure best design practices and the guidelines below are followed.

1. The RF trace should have a characteristic impedance of 50 Ω. Any standard 50 Ω RF trace (micro-strip or coplanar wave guide) may be used. The width of the 50 Ω line depends on the PCB stack, e.g., the dielectric of the PCB, dielectric constant of the material, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
2. A thicker trace allows more manufacturing tolerance while keeping a 50 Ω impedance.
3. Keep the length of the RF traces as short as possible.
4. Route RF traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
5. Maintain at least one trace-width of space between nearby GND pour and the RF trace.
6. Add GND stitches around RF traces.
7. Do not route any digital or analog signal traces between the RF traces and the reference ground.
8. Etch the GND copper underneath the antenna in all layers.
9. Follow the antenna placement as per the antenna vendor layout guidelines.
10. To evaluate transmit and receive performance like Tx power and EVM, Rx sensitivity and the like, an RF connector would be required. A suggestion is to place a 'microwave coaxial connector with switch' between RF_OUT and the antenna.
11. The RF signal after the BPF may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas.
12. Use ground pour on the top and bottom layers in the RF area with plenty of ground stitch vias. Use stitching in a staggered pattern with a minimum via spacing of 32 mil (via to via, 25-mil offset) and a maximum spacing of 100 to 150 mil. After ground flooding, terminate shapes and corners with vias to tie to other planes for improved EMI performance.

Considering the above recommendations and the placement guidelines described in the earlier section, a possible RF circuitry routing in Layer 1 is shown below. Major parts and traces are also highlighted below.

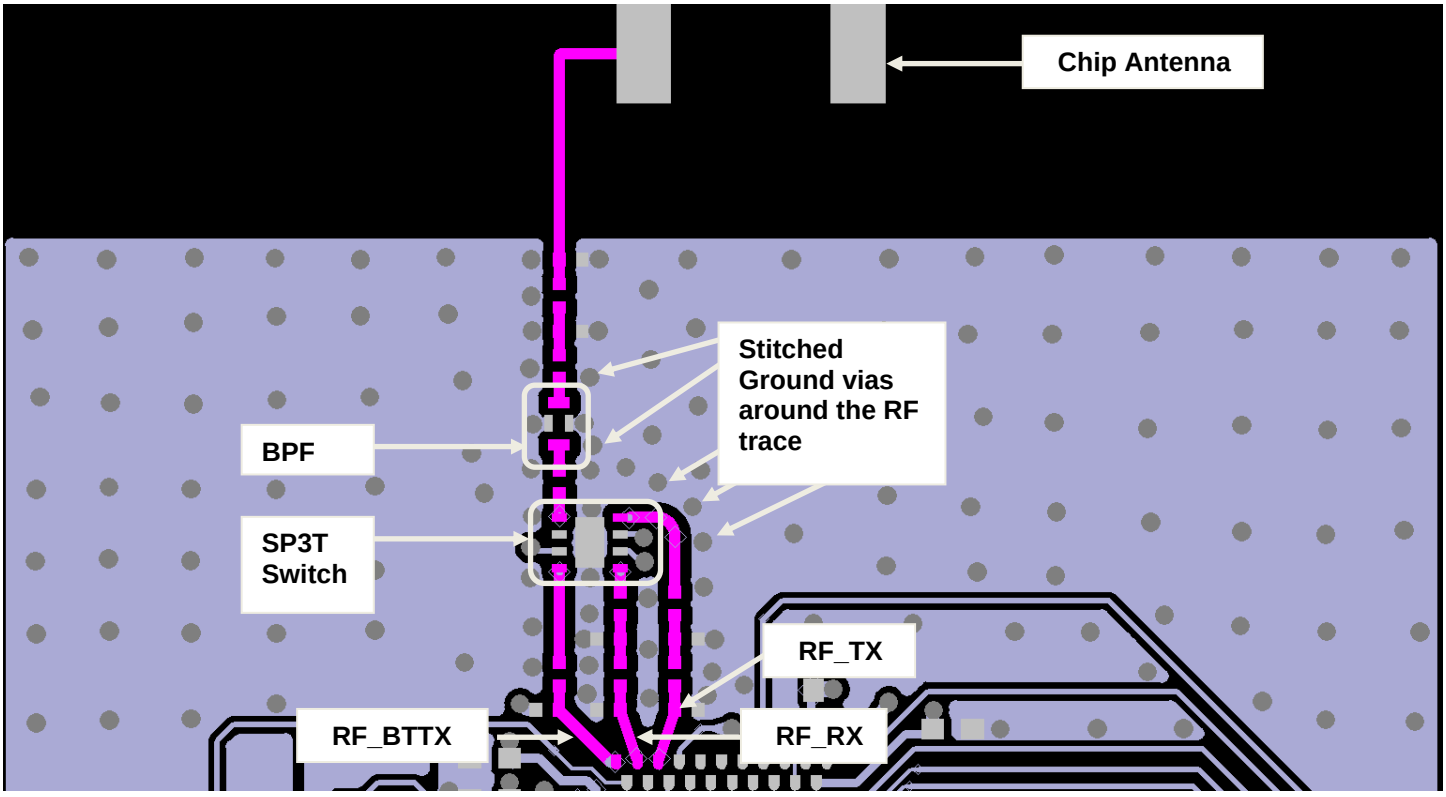

Figure 2: RF Circuitry Routing in Layer 1

The image below shows the overlap of RF routing on Top layer and the GND plane in the second layer. As can be observed, the entire RF circuitry has the second layer as GND reference. GND vias around RF circuitry are stitched directly to the GND plane.

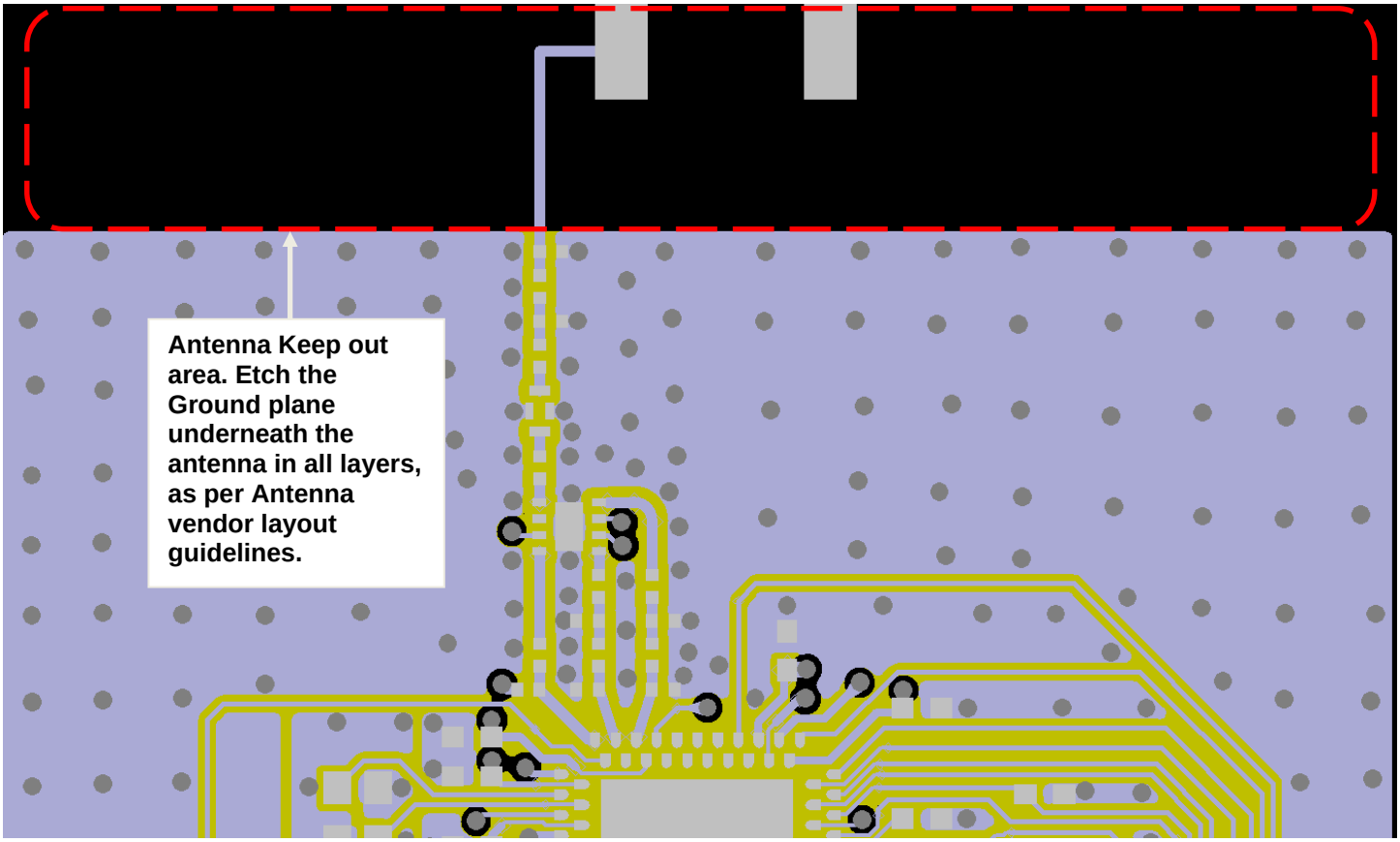

Figure 3: RF Circuitry Overlap with GND Layer

4 Crystal Layout Guidelines

Crystal placement and traces routing affect the crystal performance, and hence the start-up of the SoC after power on. The designer must ensure best design practices and guidelines below are followed.

1. Route the XTAL_IN and XTAL _OUT traces in top layer.
2. Place the XTAL as close to the SOC as possible and route these traces with shorter length.
3. Do not route the other traces underneath the XTAL lines.
4. All the non-crystal circuit traces and vias must be outside the crystal circuit area.
5. The XTAL GND pin should have a direct via to the reference GND plane.
6. It is recommended to have the GND pour around XTAL and its traces.
7. Follow the crystal part's layout guidelines.

The image below shows the crystal placement and routing in Layer 1, as an example.

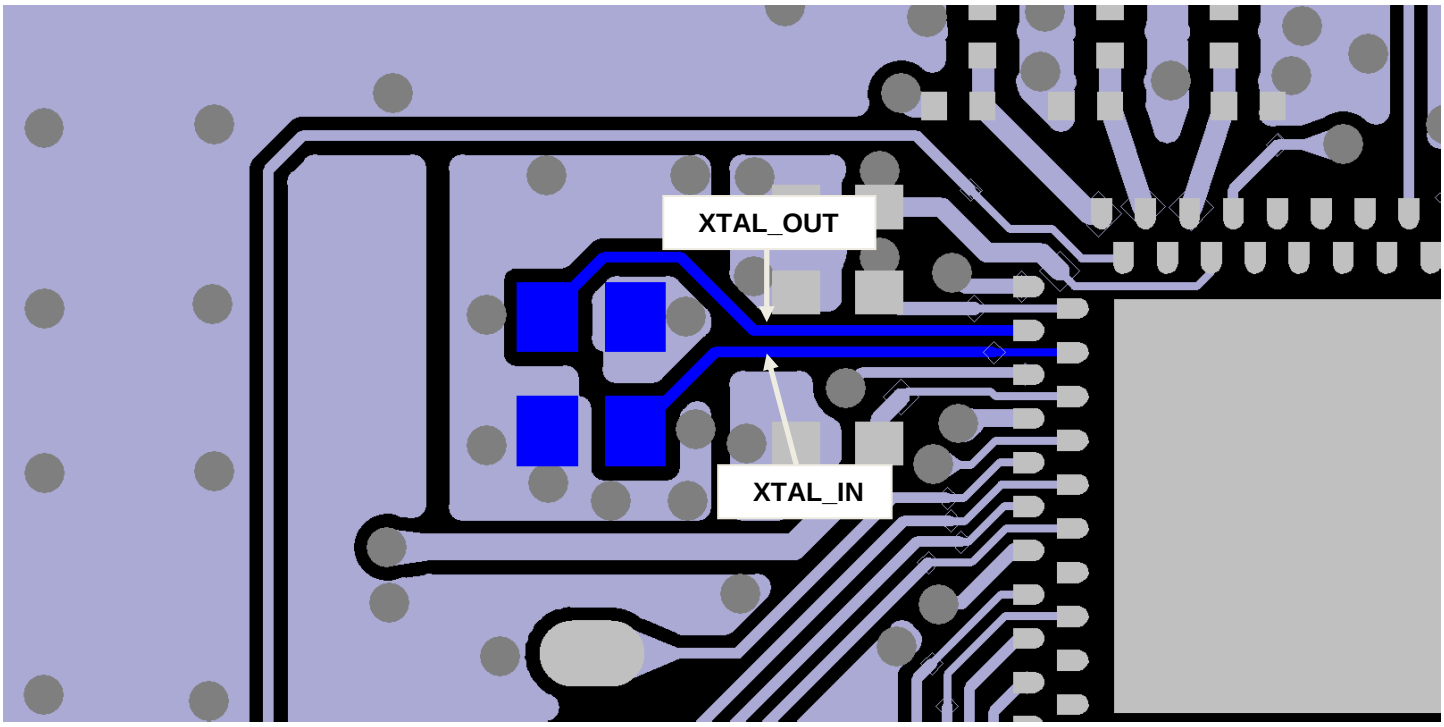

Figure 4: 40 MHz Crystal Routing in Layer 1

5 SDIO/SPI Layout Guidelines

SDIO and SPI are high speed interfaces where-in clock signals can reach up to 100 MHz. High speed design guidelines like below must be followed for the signals in these interfaces. SDIO/SPI signals include SDIO_CLK/SPI_CLK, SDIO_CMD/SPI_CSN, SDIO_D0/SPI_MOSI, SDIO_D1/SPI_MISO, SDIO_D2/SPI_INTR, SDIO_D3.

1. The characteristic impedance of the SDIO/SPI lines should be 50 Ω.
2. Match the lengths of all SDIO/SPI lines within 100 mils tolerance.
3. Keep the SDIO_CLK/SPI_CLK trace away from nearby traces with minimum 2x distance.
4. Do not route the parallel trace above or underneath the SDIO_CLK/SPI_CLK trace.
5. Keep SDIO/SPI traces away from all clock lines and noisy power supply components such as the switcher inductors. Avoid crossing over power supplies or ground discontinuities. SDIO/SPI traces should have a solid ground on the layer adjacent to them.
6. Do not leave any stubs on the SDIO/SPI traces.

The image below shows the SDIO/SPI traces routing in Layer 1, as an example. The series resistor on SDIO_CLK/SPI_CLK is placed closer to the source of this clock, rather than placing closer to QMS SoC.

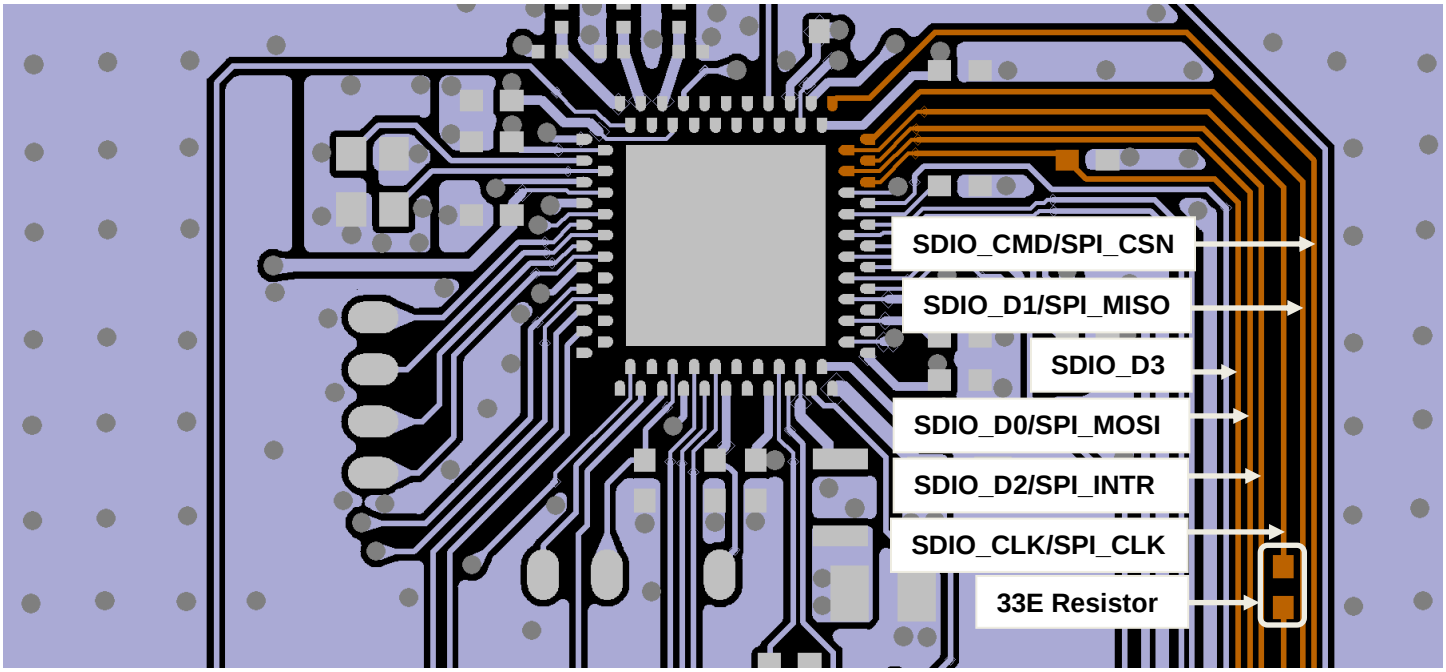

Figure 5: SDIO/SPI Signals Routing in Layer 1

6 USB Layout Guidelines

USB signals can reach speeds of 480 Mbps. Guidelines for the differential signals USB_DP and USB_DM must be followed.

1. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (say, a) that achieves 90 Ω of differential impedances and 45 Ω for each trace.
2. To minimize crosstalk between the two USB differential signals (USB_DP and USB_DN) and other signal traces routed close to them, it is recommended that a minimum spacing of 3xa be maintained for low-speed non-periodic signals and a minimum spacing of 7xa be maintained for high-speed periodic signals.
3. It is recommended that the total trace length of the signals between RS9116 part and USB connector (or USB host part) be less than 450 mm.
4. If the USB high-speed signals are routed on the Top layer, best results will be achieved if Layer 2 is a continuous Ground plane. Furthermore, there must be only one ground plane under high-speed signals and avoid the high-speed signals crossing from GND plane to another ground plane.
5. Do not route the USB differential lines close to edge of the board.

The image below shows USB differential traces routing in Layer 1, as an example.

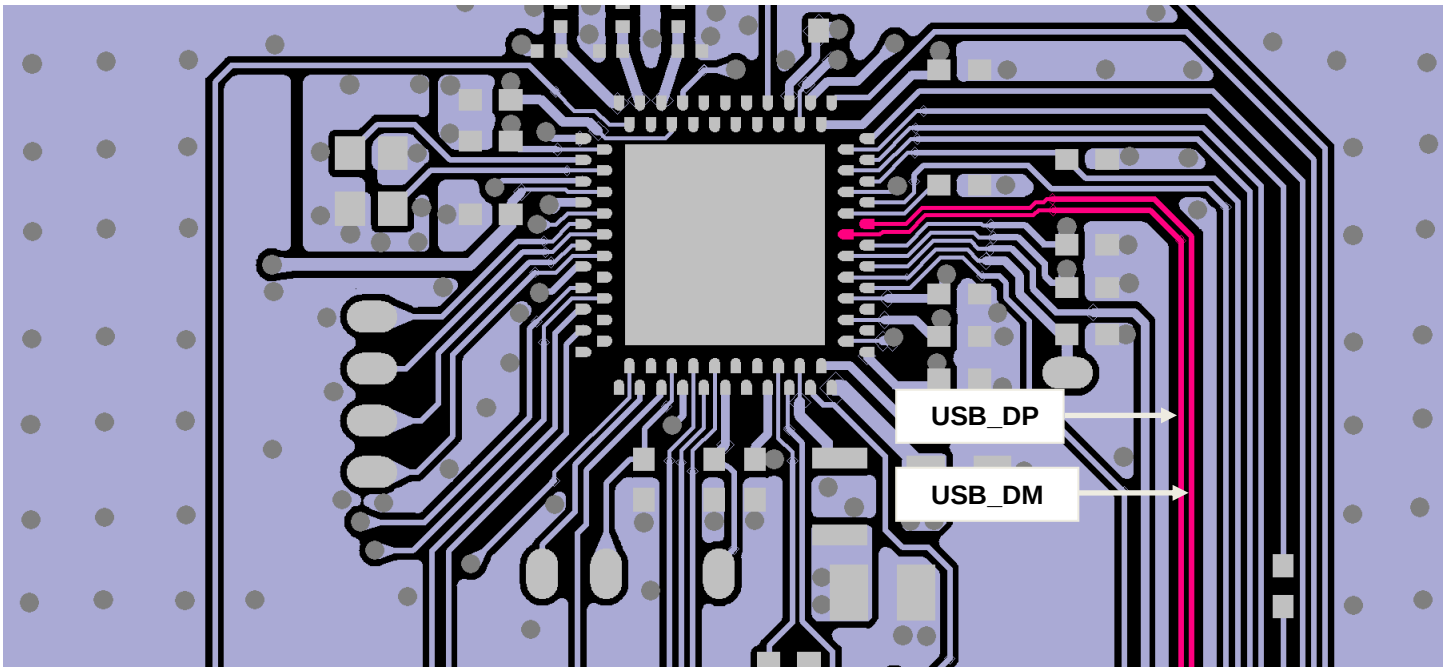

Figure 6: USB Signals Routing in Layer 1

7 UART Layout Guidelines

Below guidelines must be followed for UART signals. The signals are UART1_TX, UART1_RX, UART1_RTS, UART1_CTS.

1. Keep the UART signals away from noisy sources or other sensitive signals.
2. UART signals can be routed with multiple vias. However, ensure return path is closer to the signals.

The below image shows UART traces routing in Layer 1, as an example.

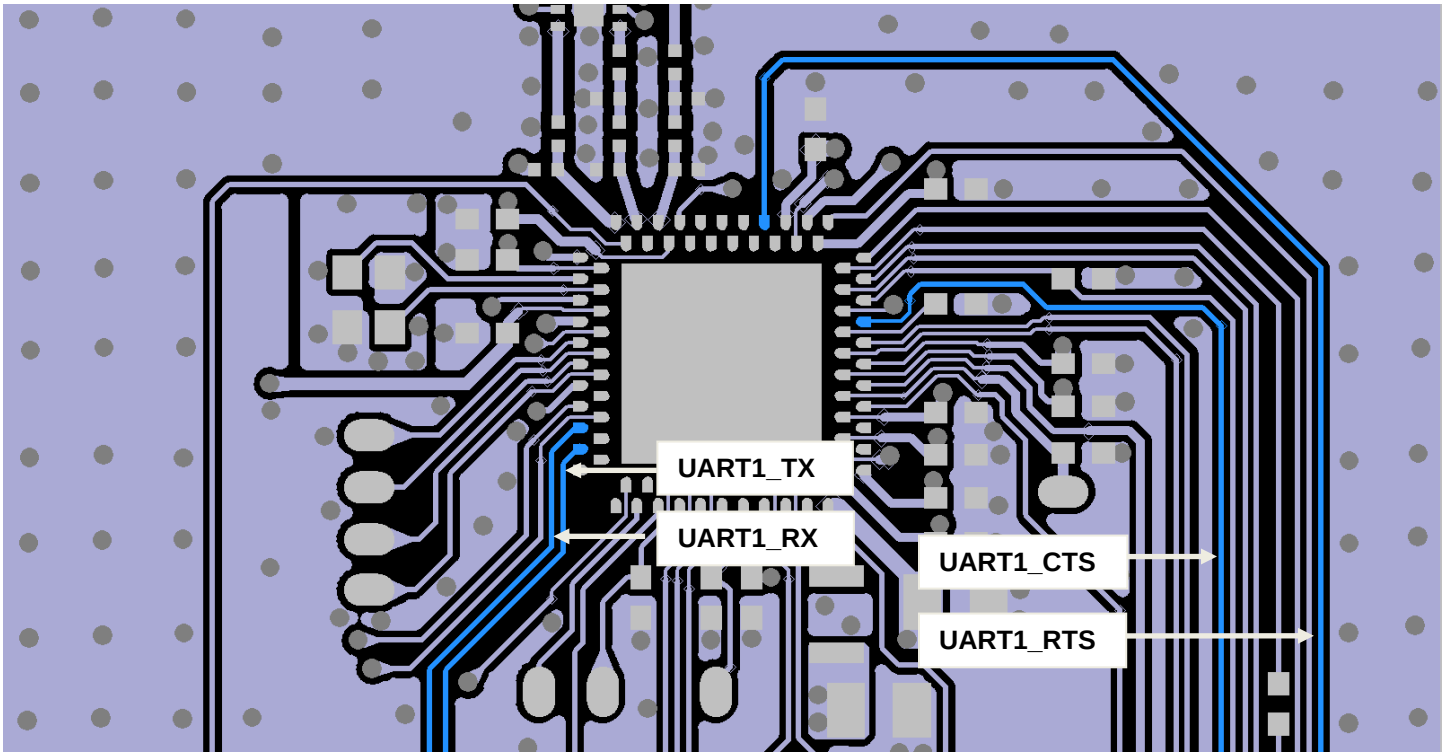

Figure 7: UART Signals Routing in Layer 1

8 Power Supply Layout Guidelines

There are many power pins on the QMS SoC. Careful routing with appropriate trace widths must be followed for better power delivery to the module. Follow the guidelines below for all the power traces.

1. The following power supply pins needs to be STAR routed from the Supply Source.
    a. VINBCKDC
    b. VINLDO1P8
    c. IO_VDD_1, IO_VDD_2
    d. ULP_IO_VDD
    e. UULP_VBATT_1
    f. UULP_VBATT_2
    g. RF_VBATT
    h. PA2G_AVDD
    i. SDIO_IO_VDD
2. The layout guidelines for the BUCK are as follows.
   Minimize the loop area formed by inductor switching node, output capacitors, and input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance and resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components.
    a. VINBCKDC Capacitor should be very close to the Chip Pin and the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    b. Buck Inductor should be close to Chip VOUTBCKDC pin and buck capacitor should be placed closer to the Inductor. The Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    c. The Ground Plane underneath the Buck Inductor in the Top Layer should be made as an isolated copper patch and should descend to the Second Layer (Main Ground) through multiple Vias.
    d. The path from VOUTBCKDC to VINLDOSOC is a high current path. The Trace should be as short & wide as possible and is recommended to run Grounded Shield Traces on either side of this High Current Trace.
    e. The Capacitor on VINLDOSOC should be very close to the Chip Pin, and the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
3. If any power supply trace or shape needs to change layers from a layer referencing (adjacent to) the top ground plane to the bottom ground plane in the stack-up or vice versa, an equal number of ground vias should be interspersed with, or placed immediately adjacent to the vias carrying the supply voltage. This minimizes noise coupling from the supply to nearby signals and other supplies.
4. The width of power traces must be minimum of 15 mils. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
5. Place decoupling capacitors near target power pins. If possible, keep them on the same side as the module to avoid inductance due to vias.

The image below shows example layout of Internal Buck regulator's Power Supply traces routing in Layer 1.

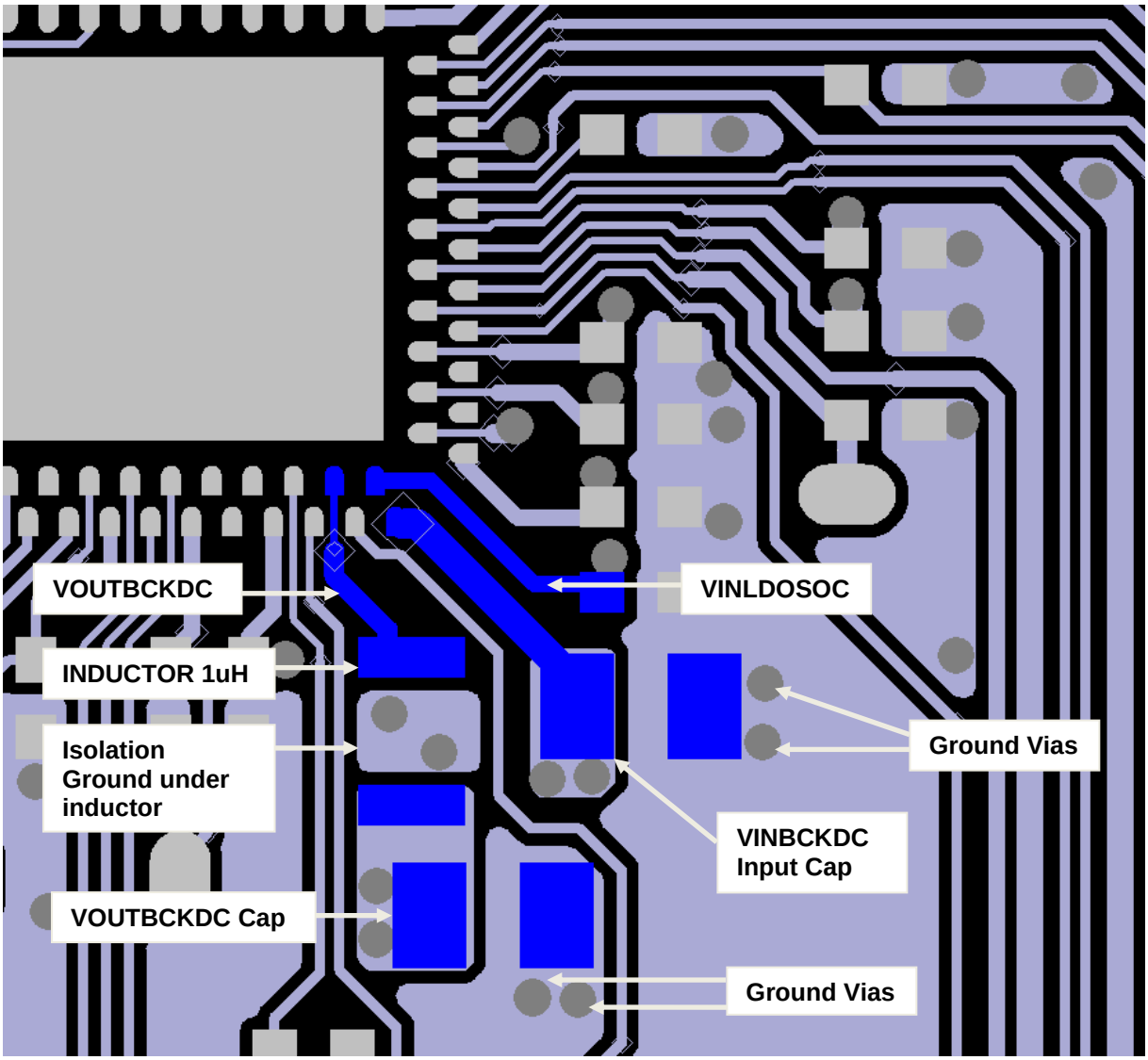

Figure 8: Internal Buck Regulator Circuitry Routing in Layer 1

The image below shows some of the Power Supply traces routing in Layer 3. As shown, they are routed in Star fashion from the supply source.

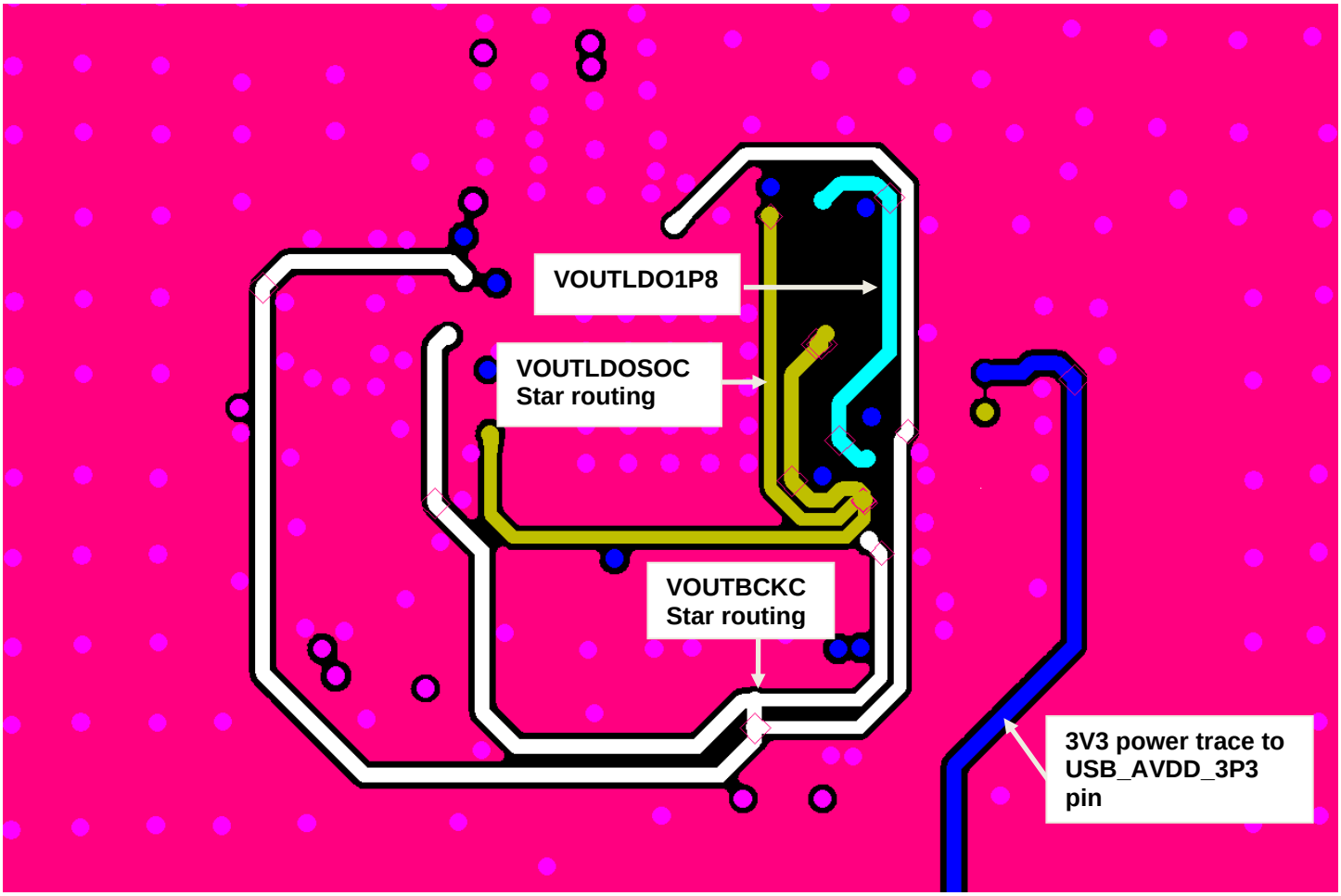

Figure 9: Power Supply Routing in Layer 3

The image below shows Power Supply traces routing in Layer 4. As shown, they are routed in Star fashion from the supply source.

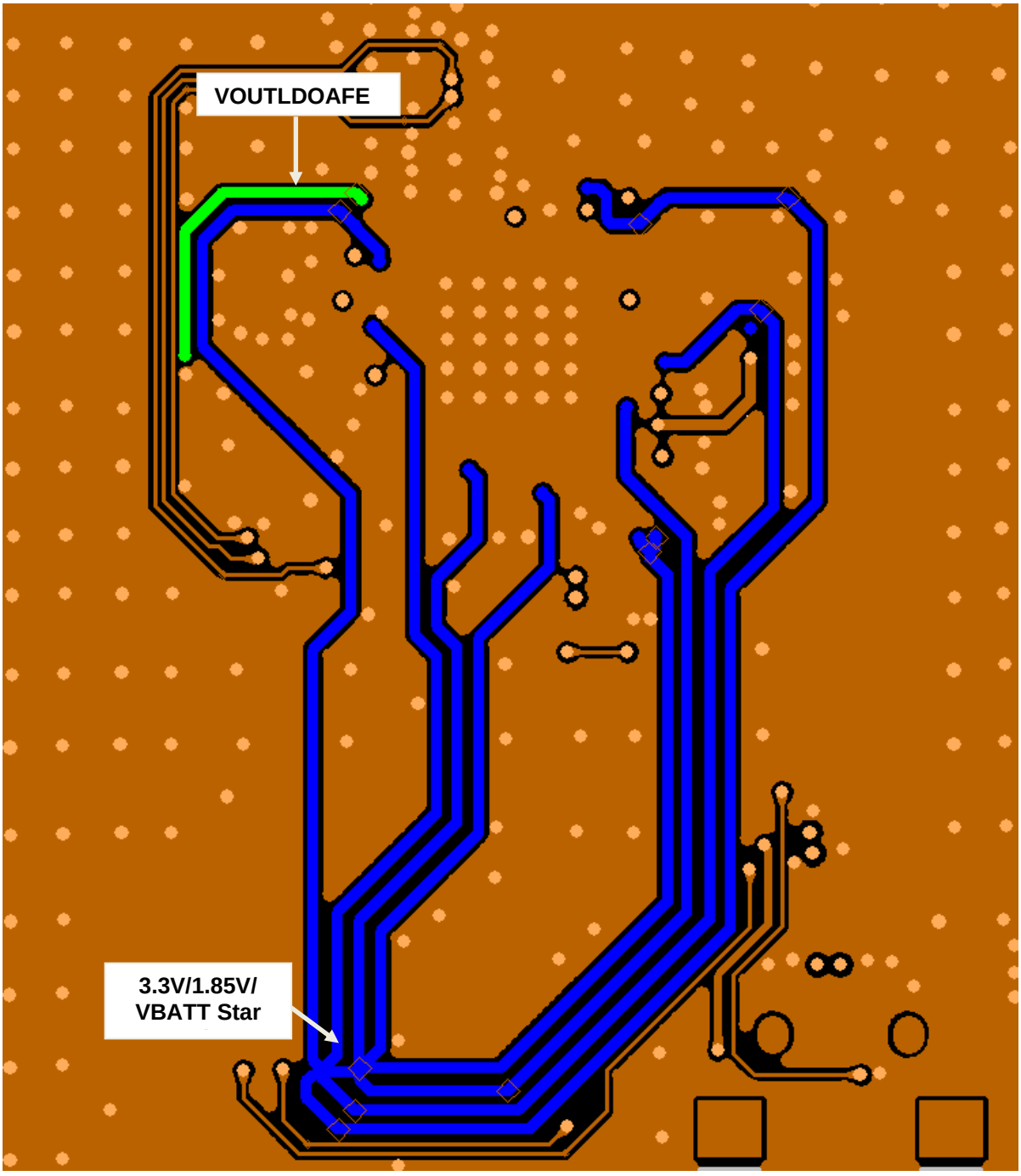

Figure 10: Power Supply Routing in Layer 4

9 GND Pour Layout Guidelines

All the returns paths of critical signals like RF, high speed signals like SPI/SDIO/USB and power, flow through GND. So, GND carries lot of return currents and high speed signals. Designer must ensure return paths are short. There are various possible ways to achieve good grounding, and below guidelines provide some of the possible insights into it.

1. Dedicate the adjacent layer of QMS SoC and its circuitry, to GND. In this document, QMS SoC and circuitry are placed in Layer 1, so Layer 2 must be completely GND plane only.
2. GND pour must be continuous with no voids.
3. Pour GND in all the empty spaces around parts and traces in all the layers. Stitch this GND pour to GND plane using multiple GND vias.
4. Avoid large GND fill without GND vias, or else it acts like an antenna, and this can possibly cause radiation of unwanted signals affecting other parts of the board. This can negatively affect board performance.

The image below shows complete GND plane in Layer 2. Also, you can observe from images in above sections, that all the empty spaces are filled with GND pour and stitched with GND vias to the GND plane.

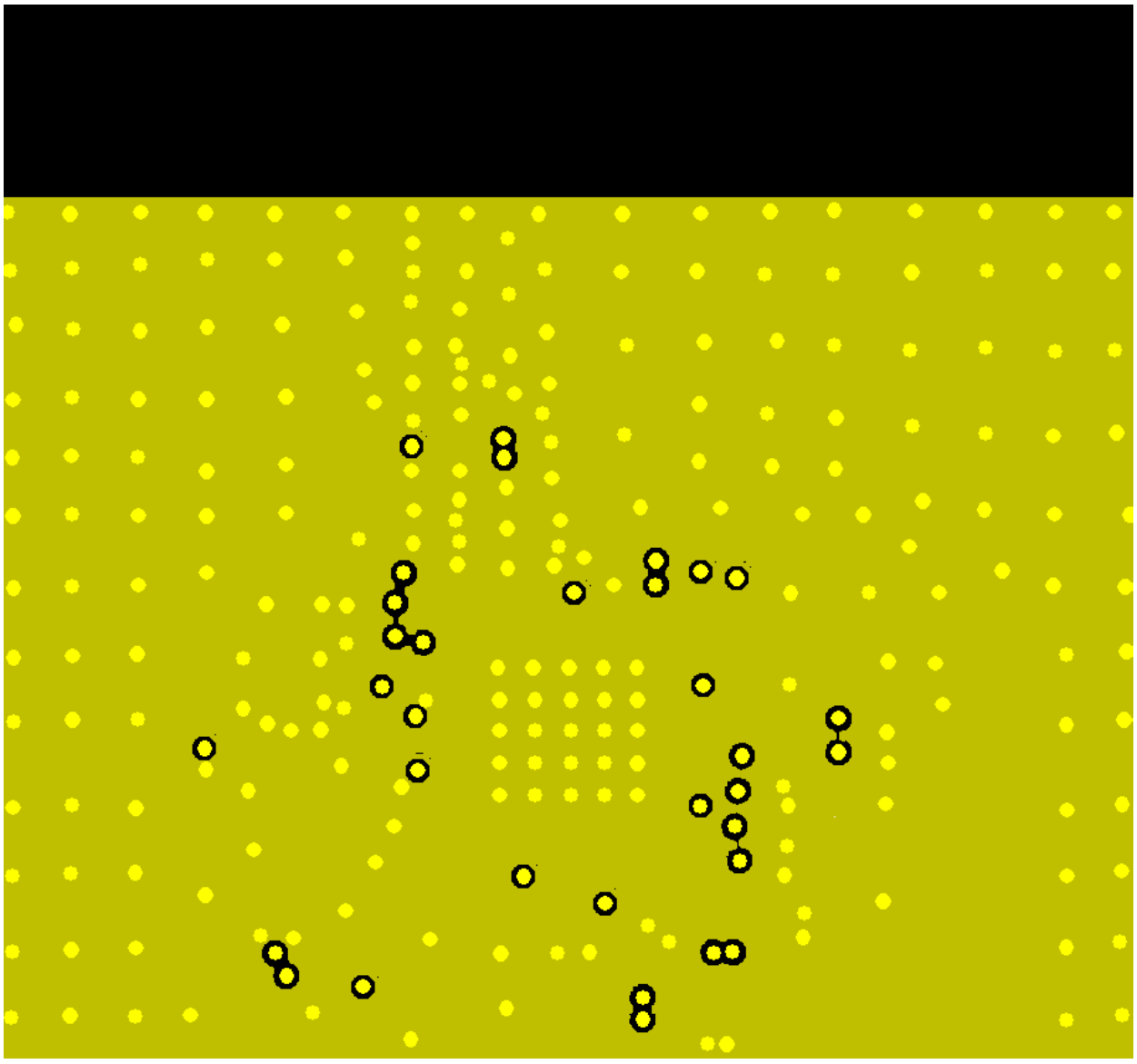

Figure 11: GND Plane in Layer 2

The image below shows the example picture of GND pour in Layer 1 with one just via. Such hanging GND pour must be avoided. Stitch GND vias near the periphery of the GND pour, or else restrict such GND pour shapes.

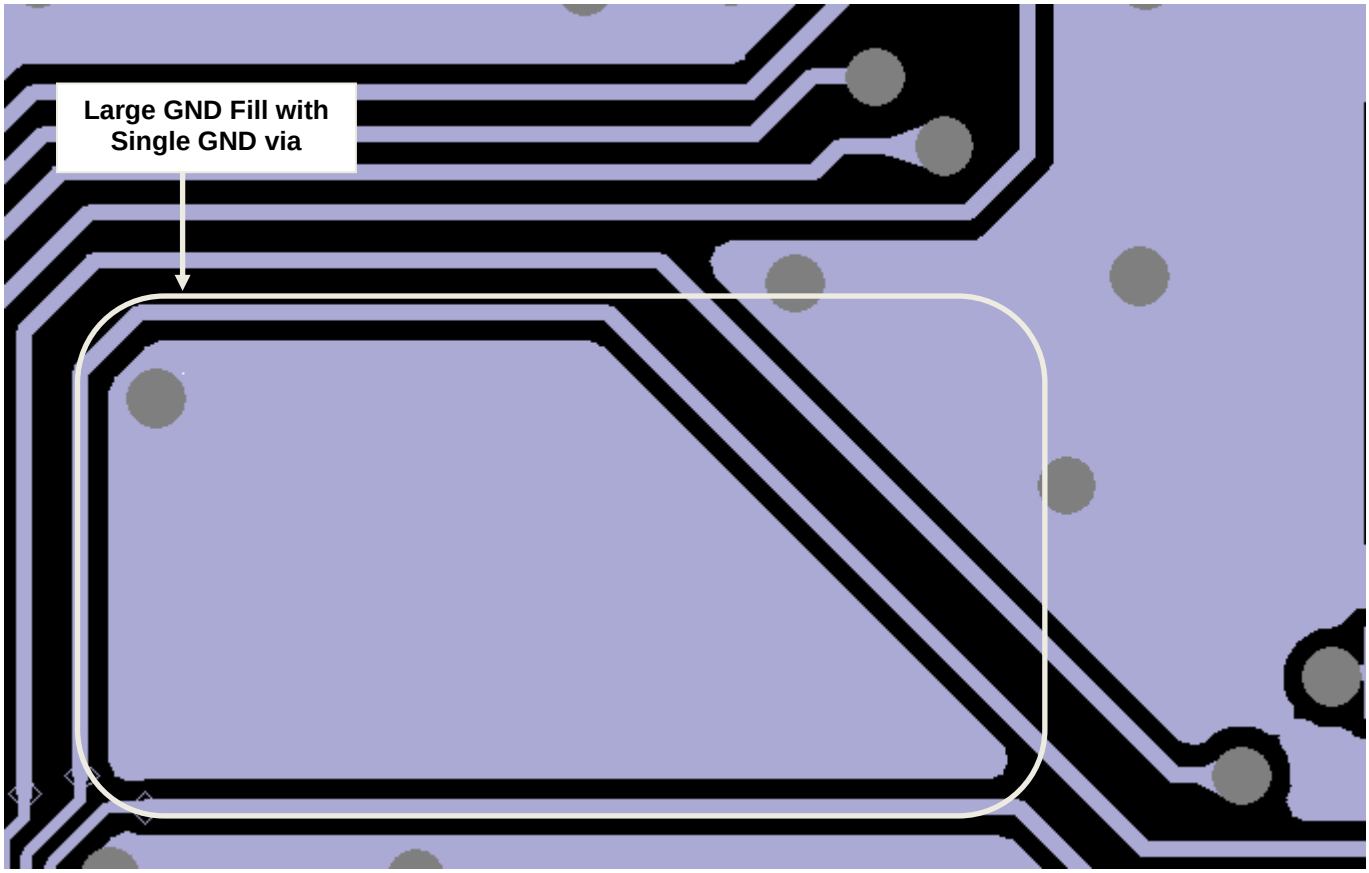

Figure 12: Hanging GND Pour

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