AN1345: RS9116 Hardware Design Checklist

Version 1.0

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1 Introduction

This document provides general RS9116 design guidelines that includes schematics and layout checklist as well as a power pin decap values table. All users should follow and adhere to the guidelines for a successful design.

2 Schematics Checklist

☐	Follow latest versions of product data sheet and documentation referenced from our website.
☐	Design follows the Reference Schematics provided in the latest data sheet, rather than following EVK design. (Use EVK for evaluation purposes only. For your design, follow the data sheet only. Do NOT follow EVK for your design)
☐	Design follows each power pin and associated capacitors as per the Reference Schematics in the data sheet. Follow Decap values for each power pin, as per the list provided in the Power Pin Decap Values section.
☐	Ferrite Beads are not recommended on RS9116 power pins.
☐	Ensure that the circuitry on the following pins meet power sequence requirements as per the data sheet : Power Supply inputs, POC_IN, RESET_N. (Some of these pins may not be available in some ICs/Modules)
☐	Check the RF performance specs and Power consumption values in the data sheet for both 3.3 V and 1.85 V supply voltages and follow the suitable supply voltage as per the application needs.
☐	Check the Power supply operating conditions for both 3.3 V and 1.85 V supply voltages as per data sheet and design the supply source(s) suitably. Ensure the supply voltage specs are meeting as per data sheet.
☐	Check that the 32 KHz clock requirements in the data sheet are adhered to in the design.
☐	Check that the Wake-up, Sleep configurations provided on some of the pins are taken care of as required. If Wake-on-wireless feature is used, a weak pull-down (Ex: 47 KΩ) is put on ULP_GPIO_6.
☐	Check that the Boot-up (Host, Internal/external flash), Programming (JTAG, ISP), Debug (UART2_TX) options available in the IC/Module are taken care of as required.
☐	Connect Test points to JP0, JP1, JP2, JNC, UART2_TX pins for future debugging purposes.
☐	Connect Test points to UULP_VOUTSCDC, UULP_VOUTSCDC_RETN, VOUTLDO1P8 pins for future debugging purposes.
☐	Check the interface(s) to be used (UART, SPI, SDIO, USB, USB-CDC) and follow the recommendations given in the data sheet: a. If SDIO is used, pull-up resistors (Ex: 47 KΩ) to be used on SDIO_CMD and Data lines as per SDIO Physical Layer specification. Series resistor (Ex: 33 Ω) must be used on SDIO_CLK near the source of this signal.
☐	b. If SPI is used, ensure SPI_CSN and SPI_CLK are not floating when the device is powered up and reset is de-asserted. Series resistor (Ex: 33 Ω) must be used on SPI_CLK near the source of this signal. Check and follow the requirement of external pull-up/down resistor (Ex: 47 KΩ) on SPI_INTR pin.
☐	c. If UART is used, ensure the inputs signals UART_RX and UART_CTS are not floating when the device is powered up and reset is de-asserted.
☐	d. If USB / USB-CDC is used, ensure USB_VBUS pin is connected to 5 V supply source.
☐	If RF circuitry is provided on-board, check the following: a. Ensure 50 Ω characteristic impedance throughout RF path.
☐	b. Design RF circuitry as per Single/Dual band requirements, and other application needs.
☐	If there are any specific reasons for not following the above recommendations (and per data sheet), check them and ensure they do not affect the functionality, performance, reliability of the module and product.

3 Layout Checklist

☐	Follow latest versions of product data sheet and documentation referenced from our website.
☐	Design follows the Layout Guidelines provided in the latest data sheet.
☐	In the PCB stack-up, GND layer (entire layer with continuous solid plane) is adjacent to RS9116 part.
	Follow the Power guidelines below:
☐	a. Star routing is used from the supply source to the power pins.
☐	b. Decaps to be placed close to the intended power pins, and the trace lengths (from decap to power pin) are as short as possible.
☐	c. If internal Buck is used, follow its components placement and routing as per the Layout guidelines in the data sheet.
☐	d. If power trace is interchanging the layers, GND vias have been placed immediately adjacent to these power traces.
☐	e. All the power traces are routed with at least 15mils width.
	If SDIO/SPI is used, follow the guidelines below:
☐	a. Series resistor (Ex: 33 Ω) on CLK is placed near the source of clock signal.
☐	b. Clock signal is away from nearby traces with minimum 2x trace width distance.
☐	c. No signal is routed in parallel to the above or underneath the clock signal.
☐	d. Length matching of its traces are done with 100mils tolerance.
☐	e. SDIO/SPI traces are away from noisy power traces.
☐	f. There are no stubs on SDIO/SPI lines.
	If USB is used, follow the guidelines below:
☐	a. Ensured 90ohm differential impedance is followed for D+ & D- lines throughout.
☐	b. D+ & D- lines are away from nearby low-speed signals with minimum 3x trace width distance; and away from high-speed signals with minimum 7x trace width distance.
☐	c. Length of USB signals is less than 450 mm from Connector/Host to RS9116.
	If RF circuitry is provided on-board, follow the guidelines below:
☐	a. RF circuitry is placed and routed in the same layer as RS9116, without any vias in the path.
☐	b. Ensure 50 Ω characteristic impedance is followed throughout RF path.
☐	c. GND vias are used all around RF path, and they are stitched directly to GND plane.
☐	d. RF trace lengths are as short as possible.
☐	e. Antenna layout guidelines from the vendor, must be followed.
☐	f. There is a continuous GND reference plane adjacent to the RF path.

	If external Flash is used, follow the guidelines below:
☐	c. Clock signal is away from nearby traces with minimum 2x trace width distance.
☐	d. Length matching of its traces are done with 100 mils tolerance.
☐	e. No signal is routed in parallel to the above or underneath the clock signal.
☐	There are no parallel traces in adjacent layers.
☐	GND vias are stitched adjacent to high speed signals vias, wherever high speed signals (like SDIO/SPI, USB) are interchanging the layers.
☐	High speed signals (like SDIO/SPI, USB) have continuous GND reference plane throughout.
☐	There are no high speed signals (like SDIO/SPI, USB) routed close to the edge of the board.
☐	If Crystal is used, follow layout guidelines from its vendor. Its traces are routed as short as possible without any vias. GND is poured all around the crystal. No traces are routed underneath the crystal lines.
☐	GND is poured underneath RS9116 as per the layout guidelines in the data sheet, and GND vias have been stitched in these pours.
☐	GND pour is done such that there are no GND islands with just a single GND via, nor they are hanging on one side. (GND pours with no vias along its edges are potential sources of interference)

4 Power Pin Decap Values

INPUT - Power Pin Name	Capacitor Value for SoC/Module Package			
	QMS	B00	CC0	CC1
VINBCKDC	10uF	10uF	10uF	
VIN_3P3				10uF
VINLDO1P8	No Capacitor	No Capacitor		
IO_VDD	0.1uF together (2 pins)	0.1uF together (4 pins)	0.1uF (1 pin)	
ULP_IO_VDD	0.1uF	0.1uF	0.1uF	0.1uF
C_VDD	No Capacitor (3 pins)	0.1uF together (3 pins)		
UULP_VBATT_1	No Capacitor	No Capacitor	No Capacitor	0.1uF
UULP_VBATT_2	1uF	1uF	1uF	
RF_VBATT	No Capacitor	No Capacitor	No Capacitor	
VINLDOSOC	0.1uF	0.1uF	0.1uF	
PA2G_AVDD	1uF (1 pin)	1uF (1 pin)	1uF (1 pin)	
PA5G_AVDD			1uF together (2 pins)	1uF (1 pin)
RF_AVDD	1uF together (3 pins)	1uF together (2 pins)	1uF (1 pin)	
FLASH_IO_VDD	No Capacitor			
SDIO_IO_VDD in RS9116	0.1uF	0.1uF	0.1uF	0.1uF
RF_AVDD33			0.1uF	0.1uF
AVDD_1P9_3P3			(0.1uF + 1uF) together (5 pins)	0.1uF (1 pin)
UULP_AVDD		0.1uF	0.1uF	0.1uF
RF_AVDD_BTTX		No Capacitor	No Capacitor	No Capacitor
AVDD_1P3		No Capacitor		
AVDD_1P2 (with 0ohm series resistor)			No Capacitor	No Capacitor
USB_AVDD_3P3	0.1uF if USB is used, else connect to GND directly			
USB_AVDD_1P1	0.1uF if USB is used, else connect to GND directly			
VOUTBCKDC	1uH* + 10uF	1uH* + 10uF	1uH* + 10uF	
VOUTLDOAFE	1uF	No Capacitor	No Capacitor	No Capacitor
AUX_AVDD	1uF			
VOUTLDO1P8	1uF		No Capacitor	No Capacitor
VOUTLDOSOC	1uF	No Capacitor	No Capacitor	No Capacitor
UULP_VOUTSCDC	2.2uF	No Capacitor	No Capacitor	No Capacitor
UULP_VOUTSCDC_RETN	1uF	No Capacitor	No Capacitor	No Capacitor

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