AN1402: RS9116 Hardware Debugging Guidelines

This document provides guidelines for debugging hardware-related issues with RS9116.

Users may encounter issues while working with RS9116-based prototypes or products. Most of these issues are simple to resolve and may require only minor fixes. Users can resolve the issues by following this set of guidelines.

KEY INFORMATION

- General Debugging Guidelines
- Issue specific Debugging Guidelines

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1 Introduction

This document covers procedures to resolve issues that users commonly encounter. It contains a few general guidelines that must be followed irrespective of the issue. The guidelines have been divided based on the severity of the issue encountered by the user, for cases when no prototype/product board is working and when a few of them are not working. There are general guidelines and issue-specific guidelines in this document. The general guidelines must be followed before proceeding with the issue-specific guidelines.

2 Debugging Test Points

This section contains information about pins that are useful for debugging. These pins have been mentioned as test points (TP) in the datasheet reference schematics.

Table 1. Descriptions of Debugging Test Points

Pin(s)	Description
UULP_VOUTSCDC	This is the LDO output voltage that will power the UULP domain. If this voltage is not as per the latest specifications in the data sheet, RS9116 will not work as intended.
UULP_VOUTSCDC_RETN	This is the LDO output voltage that helps retain the RAM contents. If this voltage is not as per the latest specifications in the data sheet, RS9116 will not work as intended.
JP0, JP1, JP2, JNC	These are the debugging pins, but they are not accessible to the user. These can be used internally within Silicon Labs for the board's debugging.
UART2_TX	This pin will output the Serial debug logs.

3 General Debugging Guidelines

Please follow these guidelines before proceeding with issue-specific guidelines.

3.1 No Boards Working

3.1.1 Debugging Procedure

1. Ensure that the design is per the latest documents (especially the data sheet) available on the website.
2. Ensure Schematics and Layout are followed as per the checklists in AN1345.
3. Measure all Output Voltages of the Module/SoC (e.g., VOUTLDOSOC, UULP_VOUTSCDC), and ensure they are generated per specifications.
4. Capture the power sequence waveform in detail (Power supply inputs, POC_IN, RESET_N). Ensure the following:
   a. Signals are meeting timing requirements as per the data sheet.
   b. There is no unintentional second reset after power-up.
   c. Noise is within 50 mVpp for these signals.
   d. Power supply input voltages are within the operating conditions mentioned in the data sheet.
5. Ensure that there are no soldering/assembly issues. Analyze X-ray images and ensure there are no power and ground shorts.
6. If using the B00 module, ensure the board follows the soldering recommendations per AN1223: LGA Manufacturing Guidance.
7. Check the MAC IDs and lot code information of the modules/SoCs.
8. Swap the modules/SoCs between working Silicon Labs EVKs and failing boards and check the functionality of both.

3.2 Few Boards Working

3.2.1 Debugging Procedure

1. Ensure the design is per the latest documents (especially the data sheet) available on the website.
2. Ensure Schematics and Layout are followed per the checklists in AN1345: RS9116 Hardware Design Checklist.
3. Swap the modules/SoCs between working and failing boards and check the functionality.
4. Ensure that there are no soldering/assembly issues. Analyze X-ray images and ensure there are no power and ground shorts.
5. If using the B00 module, ensure the board follows the soldering recommendations per AN1223: LGA Manufacturing Guidance.
6. Check the MAC IDs and lot code information of the modules/SoCs.

4 Issue-Specific Debugging Guidelines

A few issues might require additional debugging. Please follow the general guidelines and then proceed with the subsequent guidelines.

4.1 Host Interface Issues

The module is unable to communicate with the host.

4.1.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Run with a lower clock speed for SPI/SDIO host interfaces; reduce the baud rate for the UART interface and check the functionality.
3. If multiple host interfaces are used, firstly ensure that only one host interface is used after power up and tristate the other host interface. Disconnect one of the interfaces from the module and test the working of the boards.
4. Increase the time interval between VBATT and POC_IN to 100 ms and the time interval between POC_IN and RESET to 100 ms and check that the board is working.

4.2 Low Output Tx Power

The Tx power numbers are lesser than the values in the data sheet.

4.2.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Try using a higher cap (like 4.7uF, 10uF, etc.) value on the PA2G_AVDD pin and other power amplifier pins available.
3. Try using a lower cap (like 0.1uF, etc.) value on the PA2G_AVDD pin and other power amplifier pins available.
4. Check for any noise on board, as some noise may interfere with the power supply or RF area.
5. If RS9116 CC0 or CC1 is used, check if the correct RF port is selected.
6. If RS9116 QMS, B00, or CC0 is used, account for any losses in the RF path from the chip to the antenna/connector.
7. As recommended, add an 8.2pF DC blocking cap on the RF path.
8. Ensure that the tuning circuitry matches the antenna used.
9. Measure the conducted RF power near a test point placed before the antenna. To measure conducted RF power (in Spectrum Analyzer), ensure the RF wiring on-board is done appropriately, and remove tuning circuitry and antenna from the RF path. If the conducted RF power is as expected, the issue could be due to tuning circuitry or the antenna itself.

4.3 Poor Connectivity Range

4.3.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Check sniffer captures to identify Tx/Rx issues.
3. As recommended, add an 8.2pF DC blocking cap on the RF path.
4. Ensure that the tuning circuitry matches the antenna used.
5. Check the Tx powers and Rx sensitivity in PER mode and compare the values with the data sheet.

6. Measure the conducted RF power near a test point placed before the antenna. To measure conducted RF power (in Spectrum Analyzer), ensure the RF wiring on-board is done appropriately, and remove tuning circuitry and antenna from the RF path. If the conducted RF power is as expected, the issue could be due to tuning circuitry or the antenna itself.

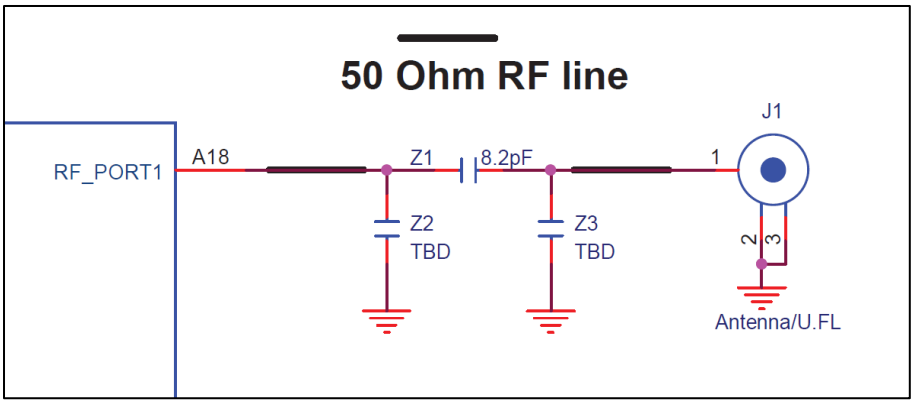

Figure 1. Recommendations for Circuitry on RF PORT as per Reference Schematics

4.4 QMS(Q7) RF Issues

1. The RS9116 QMS module is unable to join or scan an access point.
2. The RS9116 QMS module has RF frequency offset issues.

4.4.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Check if there is any noise on board, as some noise may interfere with the power supply or RF area.
3. Check crystal calibration; refer to AN1336: QMS Calibration Guide for detailed information.
4. Ensure the RF frequency variation is within 20ppm (IEEE standard).

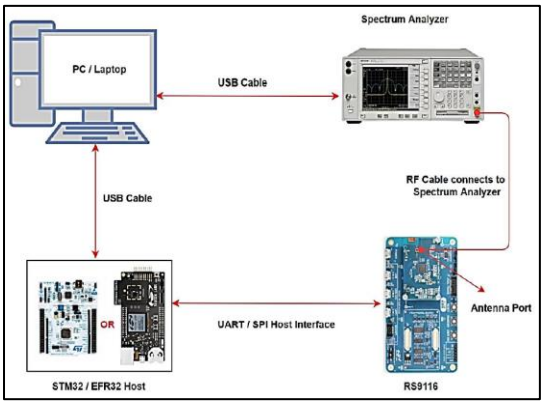

Figure 2. Crystal Calibration Setup for QMS

4.5 Access Point (AP)/Station Mode Related Issues

1. AP Mode: AP Discovery Issues
2. Station Mode: Joining/Scanning issues

4.5.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Measure the supply voltage on the PA2G_AVDD pin and ensure it is not noisy.
3. Try using a higher cap (like 4.7uF, 10uF, etc.) value on the PA2G_AVDD pin and other power amplifier pins available.
4. Try using a lower cap (like 0.1uF, etc.) value on the PA2G_AVDD pin and other power amplifier pins available.
5. Check for any noise on board, as some noise may interfere with the power supply or RF area.
6. Ensure there are no software configuration issues.

4.6 Module Overheating Issue

4.6.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Ensure there are no soldering or assembly issues on your board, and ensure the RS9116 module/SoC is soldered as per the recommendations.
3. Lower the throughput of the module and check the working. Sometimes, higher throughput may cause heating issues.
4. Check the current consumption and ensure the values are within the ones mentioned in the data sheet.
5. Check sniffer captures to identify Tx/Rx issues.
6. Check the Tx powers and Rx sensitivity in PER mode and compare the values with the data sheet.

4.7 Module Not Working at Low Temperatures

4.7.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. If using firmware earlier than v2.4, note that this issue has been fixed in the latest firmware. Contact Silicon Labs for more information.
3. Ensure parts used on board with RS9116 are rated for the operating temperature.

4.8 Module Not Working at High Temperatures

4.8.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Ensure parts used on board with RS9116 are rated for the operating temperature.
3. Lower the throughput of the module and check the working. Sometimes, higher throughput may cause heating issues.

4.9 High Current Consumption in Active Mode of the Module

4.9.1 Debugging Procedure

1. Ensure all general debugging guidelines are followed.
2. Ensure all input signals work at the same voltage level as their IO supply domain. For example,
   a. The RESET_N signal should be at 3.3V only if UULP_VBATT_1 is connected to 3.3V.
   b. The SDIO signals should be at 3.3V if SDIO_IO_VDD is connected to 3.3V.

5 References

Application Notes

Data Sheets

Schematics and Design files

AT Commands Reference