CMP101

MCU Architectures and Considerations Shaping IoT Designs

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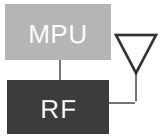
Bandwidth and Compute Are Correlated

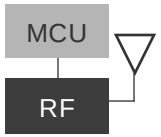
Systems have one of three architectures

Big digital plus wireless co-processor



The application processor (MPU) runs large operating system and customer applications. Wireless chip runs the wireless stack.

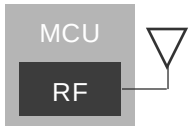
Little digital plus wireless co-processor



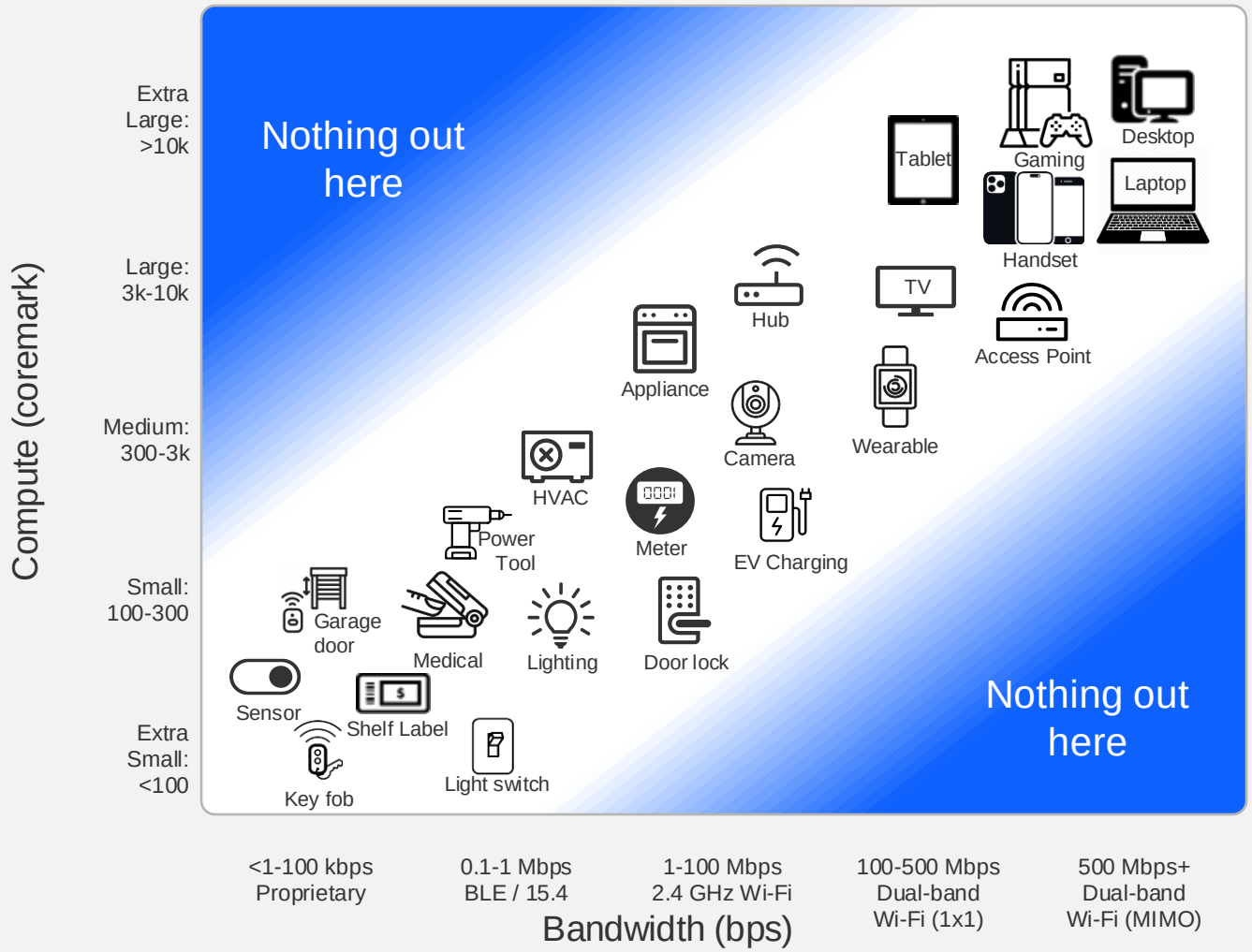
The application processor (MCU) runs bare metal or with light real-time operating system and customer applications. Wireless chip runs the wireless stack.

Key Market Trend: Power, Cost & form factor advantages, reduced complexity

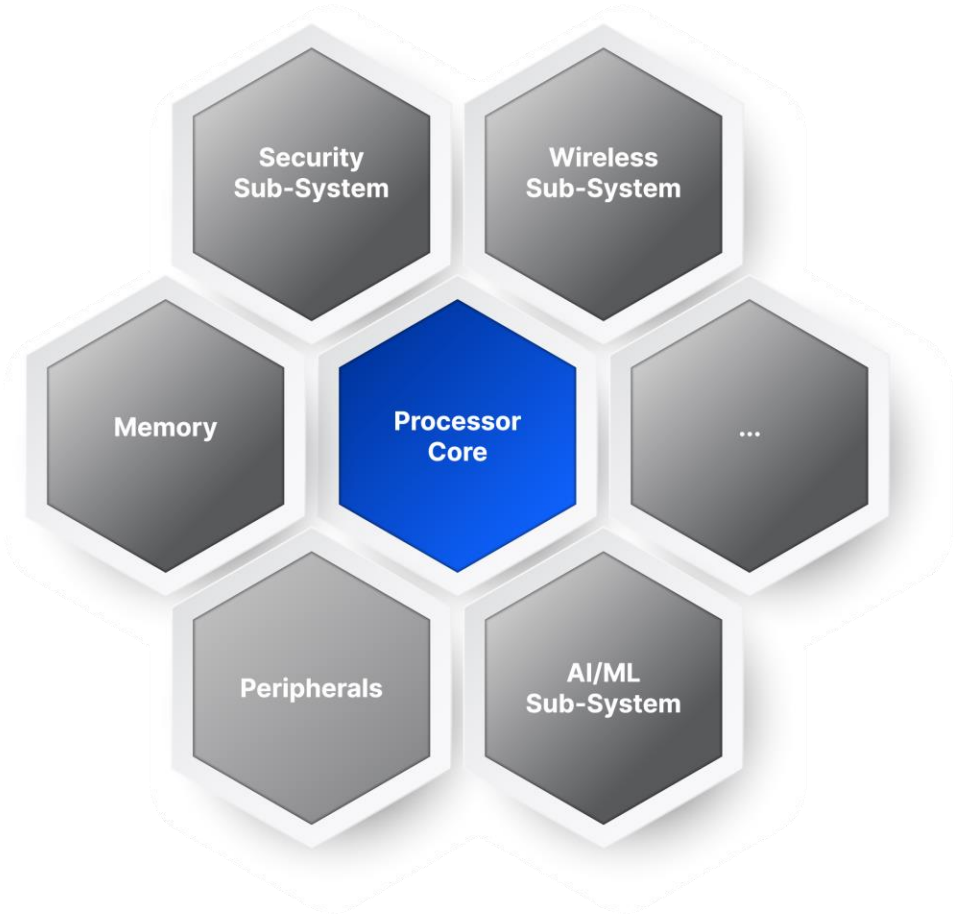
One system SoC



There is only one chip in the system. It runs both the application software and the complete wireless connectivity solution.



Building the IoT Solution



Sub-systems create building blocks for today's scalable MCU architectures

- All MCUs have 3 common subsystems:
  - Processor Core
  - Memory
  - Peripherals

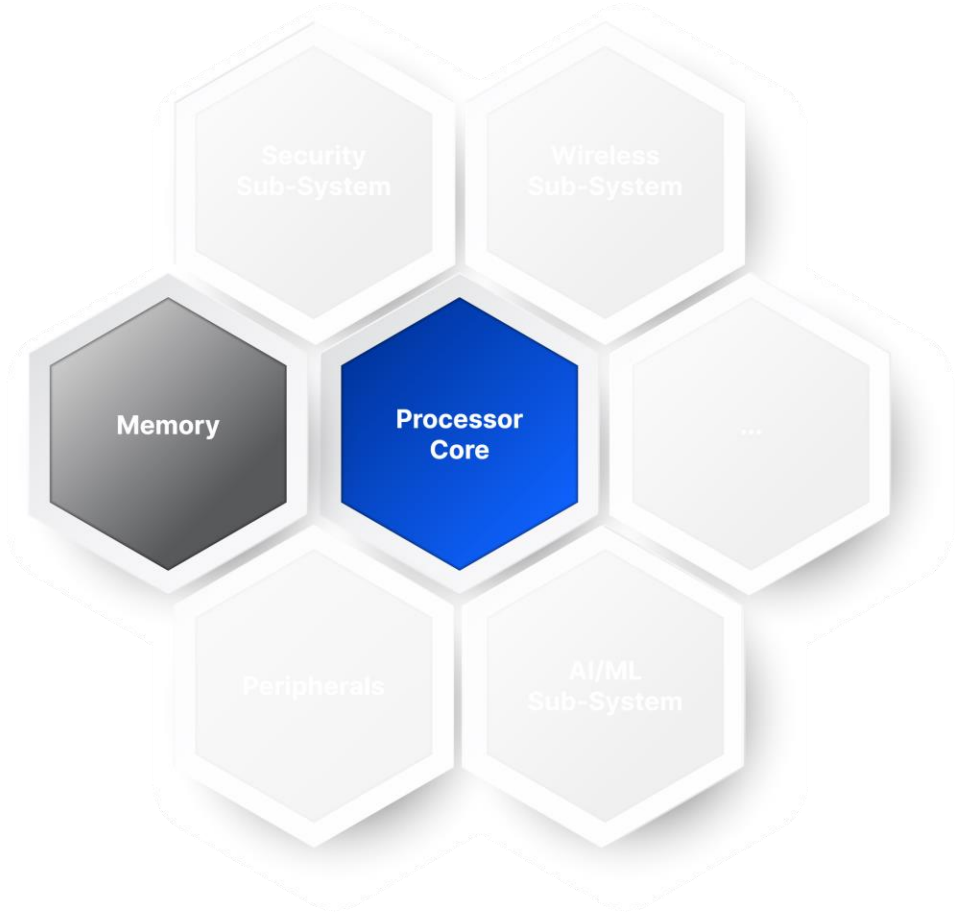
Additional Sub-systems can be added to increase functionality

- Wireless
- Security
- AI/ML
- …

Commonality between platforms simplifies developer journey

- Allows for reuse between MCU families and end-product designs

Momentum for Multi-Core



More complex systems require dedicated processor resources

- Strict timing or security requirements drive need for more diverse processor architectures
- Sub-system specific memory resources reduce overall system latency

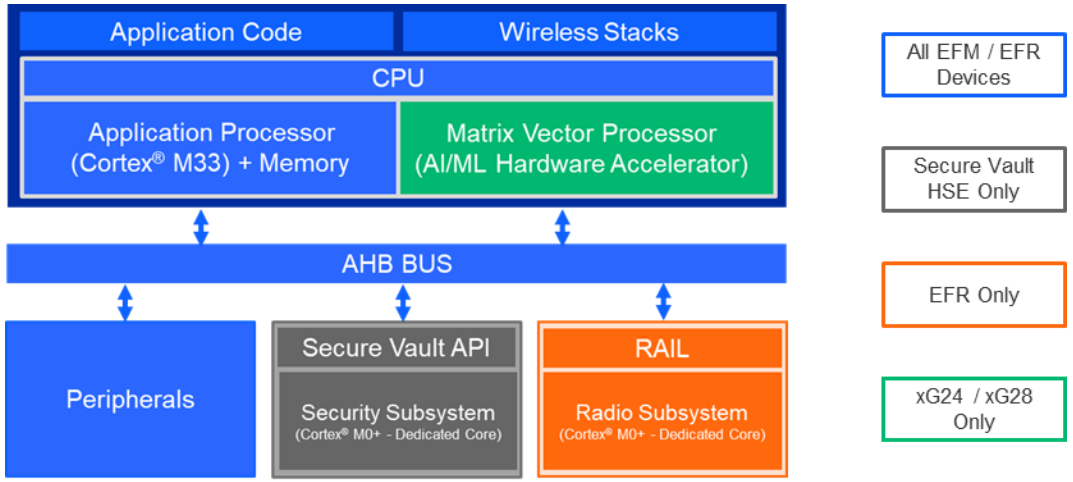
Captive cores simplify overall application development

- Dedicated sub-system processing resources allow for simplified interfaces between critical functions
- Allows for tighter control over operationally critical code for specific functions

Growing need for RTOS to manage multi-core architectures

- More complex hardware architectures limit the feasibility of bare metal implementations
- Provides code commonality across hardware platforms

A Common Platform for Connected and Non-connected Devices



Multi-Core Architecture frees up application core cycles for wireless stacks and applications

- Cortex M33 Application core for wireless stacks and application development
- Captive cores for AI/ML, Security, and Wireless sub-systems increase design flexibility

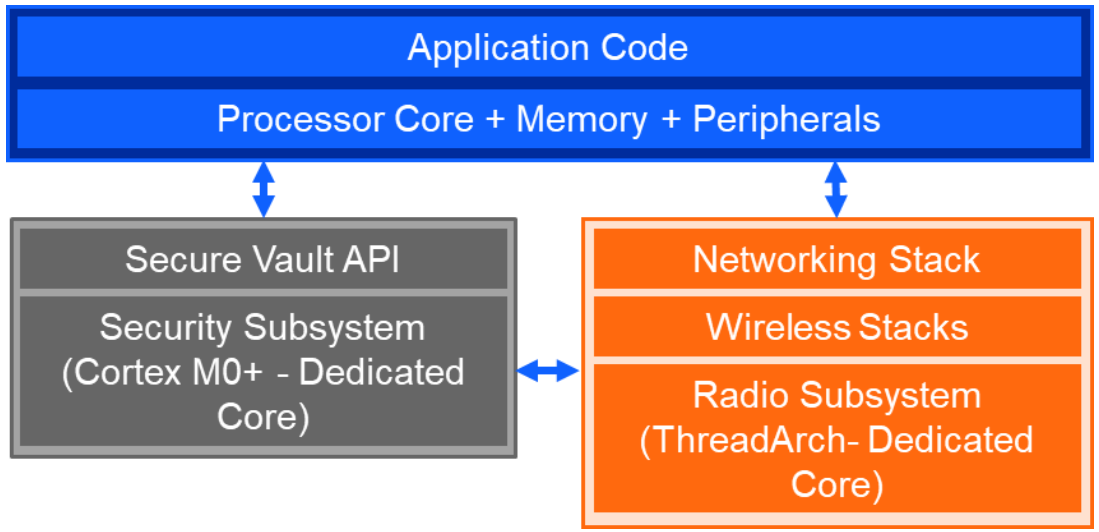
Subsystem abstraction allows developers to focus on their application

- Common security sub-system allows for design consistency across all device families
- AI/ML Hardware Accelerator improves performance and eases algorithm reuse

Flexible peripheral architectures and power modes optimize low power performance without sacrificing system performance

- Peripherals can interact autonomously allowing the application core to remain asleep longer
- Sub-system approach allows for optimized low power modes depending on use case

Multi-Core Wi-Fi SoCs Optimized for Low Power



SiWx917 benefits from differentiated architecture

- True multi-core architecture with Cortex M4 application core and proprietary network processor

Network core handles all wireless stacks, networking stack and manages Radio Sub-system

- Simplifies co-existence and manages complex timing challenges

Application core fully available for end-product development

- More processor resources available for customer application

Allows for optimized low power operation

- Can manage sleep states of both cores to extend battery life

Silicon Labs Series 3: Guiding the IoT Evolution

Improved processor performance to meet next generation challenges

- Single and multi-application core architectures along with captive cores create flexible platform for IoT development

Improved radio sub-system creates world's most flexible IoT modem

- Operate on 3 wireless networks with microsecond channel switching for true concurrency

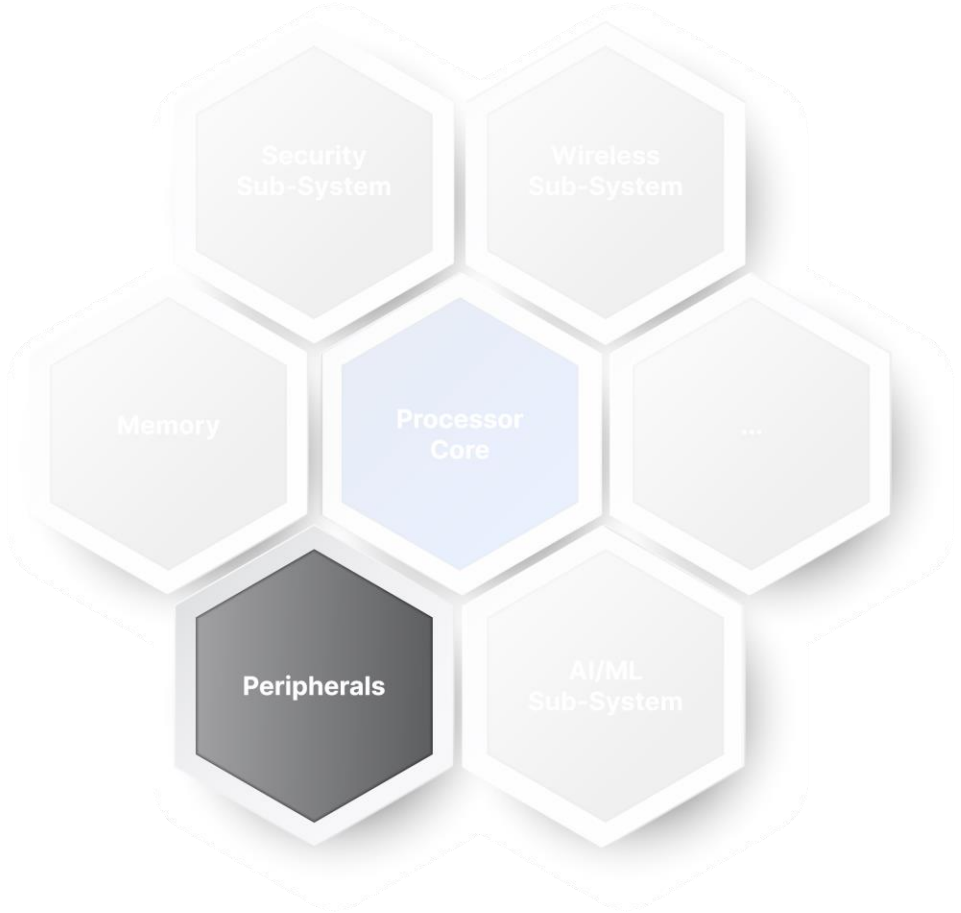
Secure Vault™ High with additional features continues to lead the way in security

- Secure memory interface hardens against primary attack vector with features like Authenticated Execute in Place

Next generation Matrix Vector Processor improves accelerated AI/ML performance

- Increases ML performance by 100x drastically reducing power consumption

Peripherals



Drive to more integrated solutions requires more advanced peripheral integration

- Application specific subsystems being created to replace external ICs

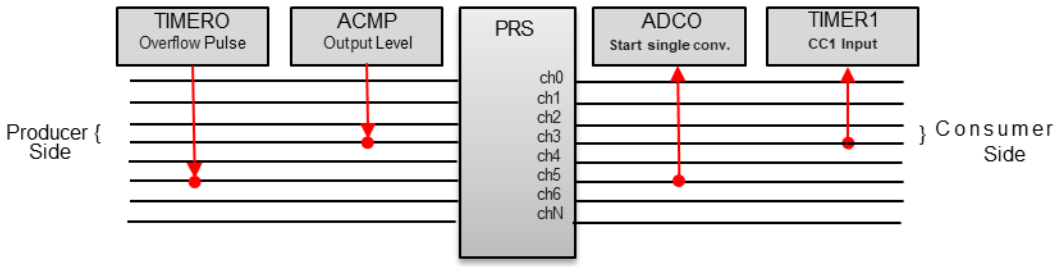
Higher speed digital peripherals migrating from MPU to MCU

- MCUs integrating complex digital subsystems to address this need

Increasing need for digital interfaces coincides with move to smaller process geometries

- Smaller process geometries increase digital performance provide but limit analog possibilities

Increased Peripheral Flexibility for Evolving Designs



PRS Block Diagram

Figure shows four peripherals connected to Two PRS channels. One channel is connected to Timer0 & ADC0 and the ACMP & Timer1 are connected to a second channel. An overflow from Timer0 can start an ADC single conversion and the ACMP output can be used as input for a compare/Capture channel on Timer1.

Peripheral Reflex System optimizes low power performance while lowering latency

- Allows for event driven peripheral interaction without burdening application core
- Processor core can stay asleep for longer and wake up only when truly needed

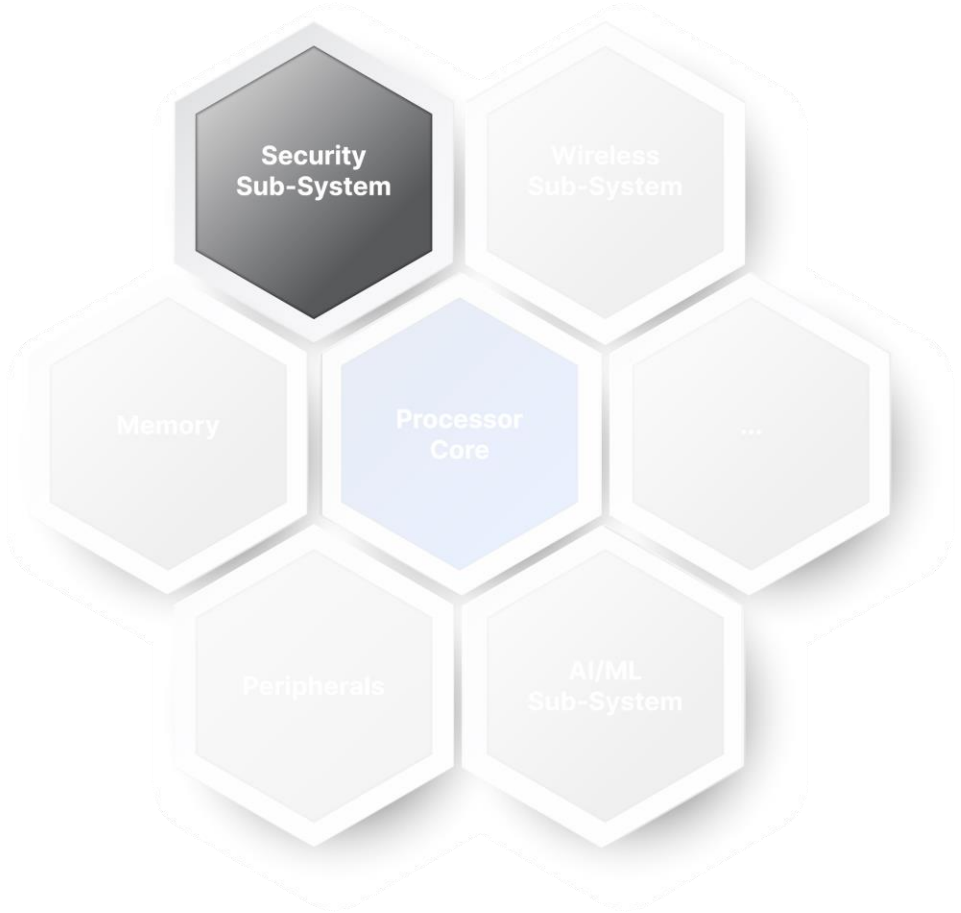
Increased peripheral integration with Silicon Labs Series 2 and Series 3

- Increased analog performance for better overall system integration
- Expansion of digital peripheral options to include more communication, memory, and sensor interfaces

More specialized sub-system peripherals simplifies architectural decisions

- Hardware acceleration and specialized interfaces for things like cameras or motor control simplify hardware and firmware architectures

Addressing Emerging IoT Security Threats



Targets are moving from IT to OT

- Companies are becoming targets rather than individuals due to greater potential rewards

Attackers are taking advantage of unsecure IoT devices

- End devices are attacked locally and used to gain access to higher level servers to get access to critical data

Worldwide legislation and standardization driving security further into IoT devices

- Local and regional standards are shaping what is required of IoT devices

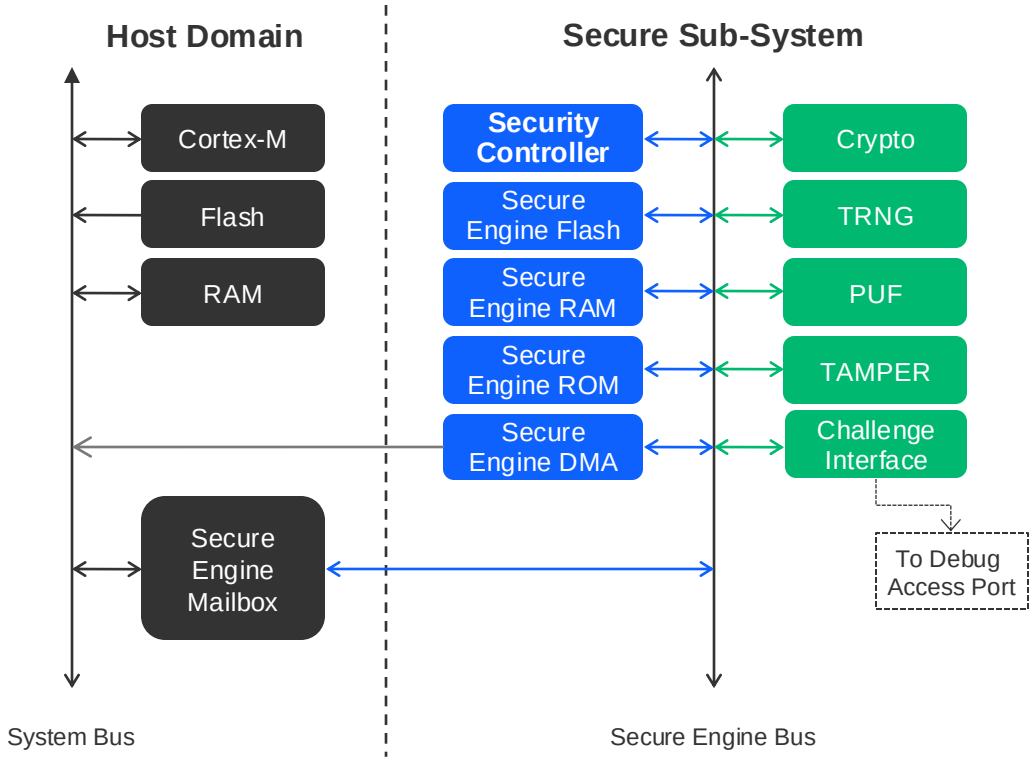
Ecosystems requiring higher levels of security than ever before

- Matter has raised the bar for security in all IoT devices

Expanding interoperability increases needs for more secure end devices

- Single vendor, single purpose networks are moving to a more open structure

Secure Vault™ – Leading Edge IoT Security



Flexible security architecture with captive Cortex M0+ core to offload application core

- Common security API allows for use across multiple IC families and protocols

All cryptographic and security functions isolated from application

- Only accessible via host mailbox or debug
- Maintains higher levels of security without compromising performance

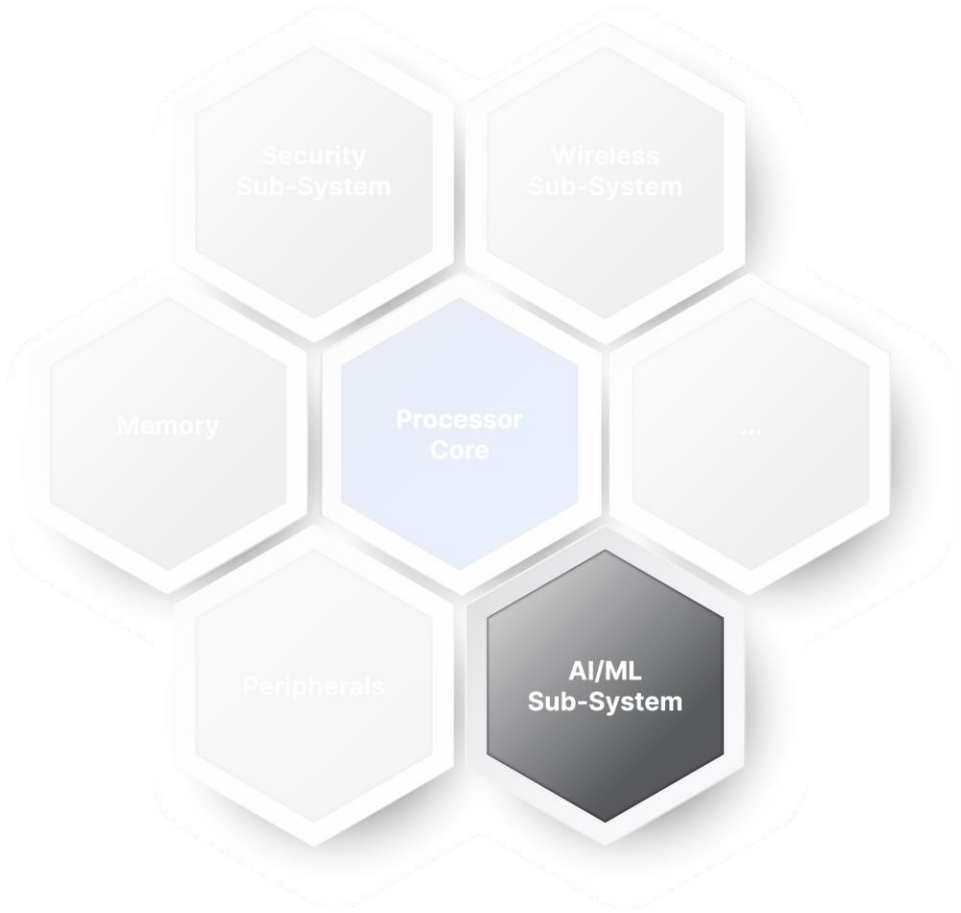
Addresses most common and emerging security threats for IoT devices

- Protects against current threats while also providing flexibility to address future challenges

Scalable architecture with Vault Mid and Vault High options

- Can select best architecture to meet today's needs while maintaining flexibility

Driving Better Localized Intelligence



Increasing need for more real-time decision making

- Faster action on data results in better, more accurate inferencing

Keep data more secure by eliminating need to transfer before processing

- Keep private data directly where decisions are being made without exposing to potential threats

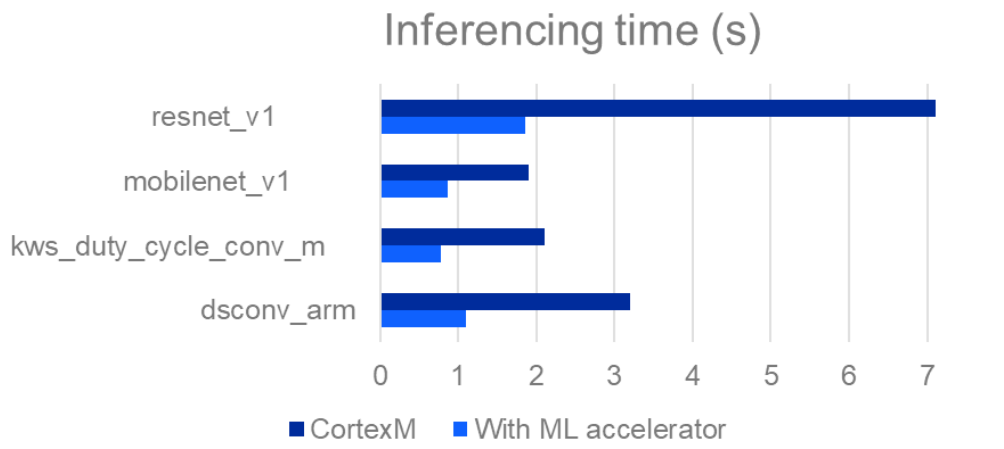
Lower deployment and recurring costs

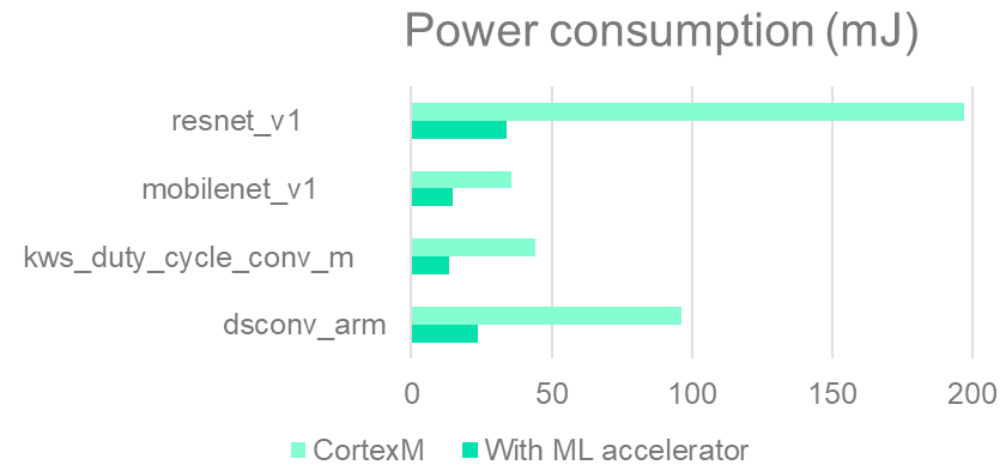
- Localization of inferencing removes dependency on costly infrastructure and data transmission

Increasing demands on processors for edge devices

- Growing need for edge intelligence is driving device makers to make compromises for power and performance

Accelerating AI/ML for the Edge





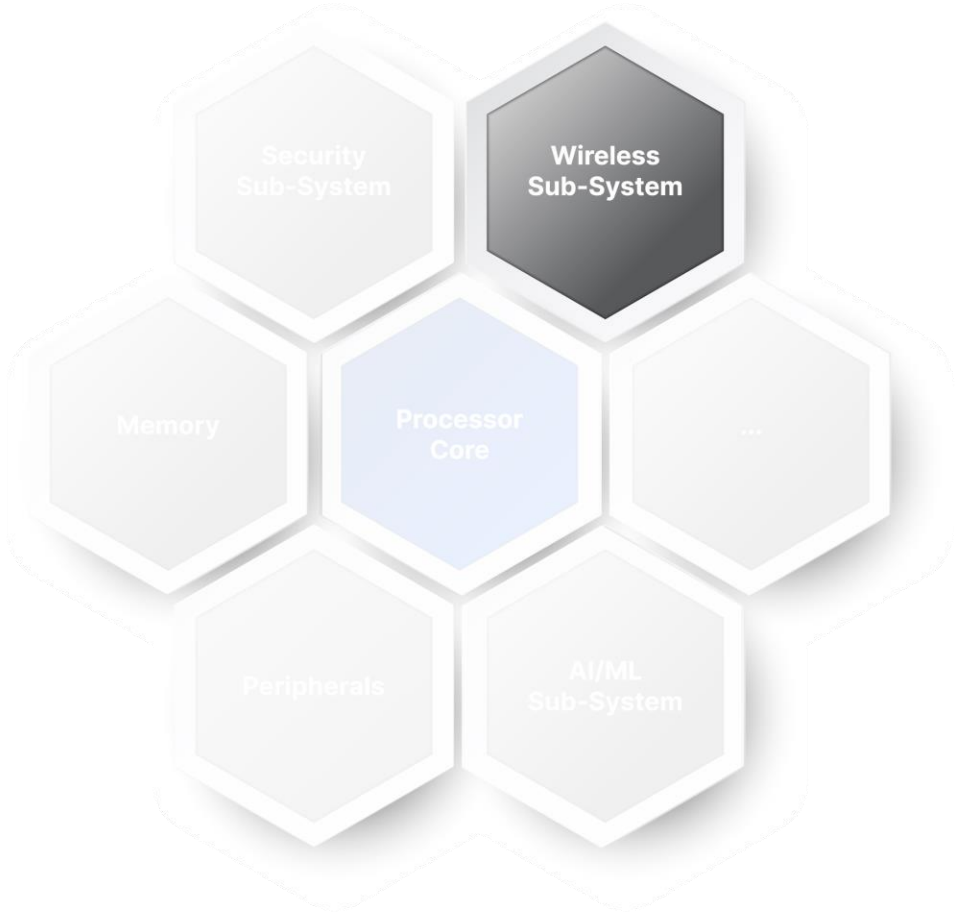
AI/ML Hardware Accelerator

- Ability to run ML inferencing more efficiently with up to 6x faster and 8x lower power compared to non-accelerated ARM Core
- Offloads application core reducing inferencing latency

Tools and partnerships to simplify algorithm development and characterization

- Silicon Labs ML Toolkit for end to end development
- Partnerships with SensiML, TensorFlow provide simple path to algorithm development and deployment
- Gecko SDK support for TensorFlow Lite Micro simplifying the ML application development
- Providing flexibility to adapt to different types of users and their workflow.
- Availability of a comprehensive library of sample codes for ML SoCs, suitable for various applications.

Simplifying and Integrating RF Designs



Integration of RF along with MCU lowers system cost and simplifies product architecture

- Fewer external components and interfaces allows for more consolidated designs

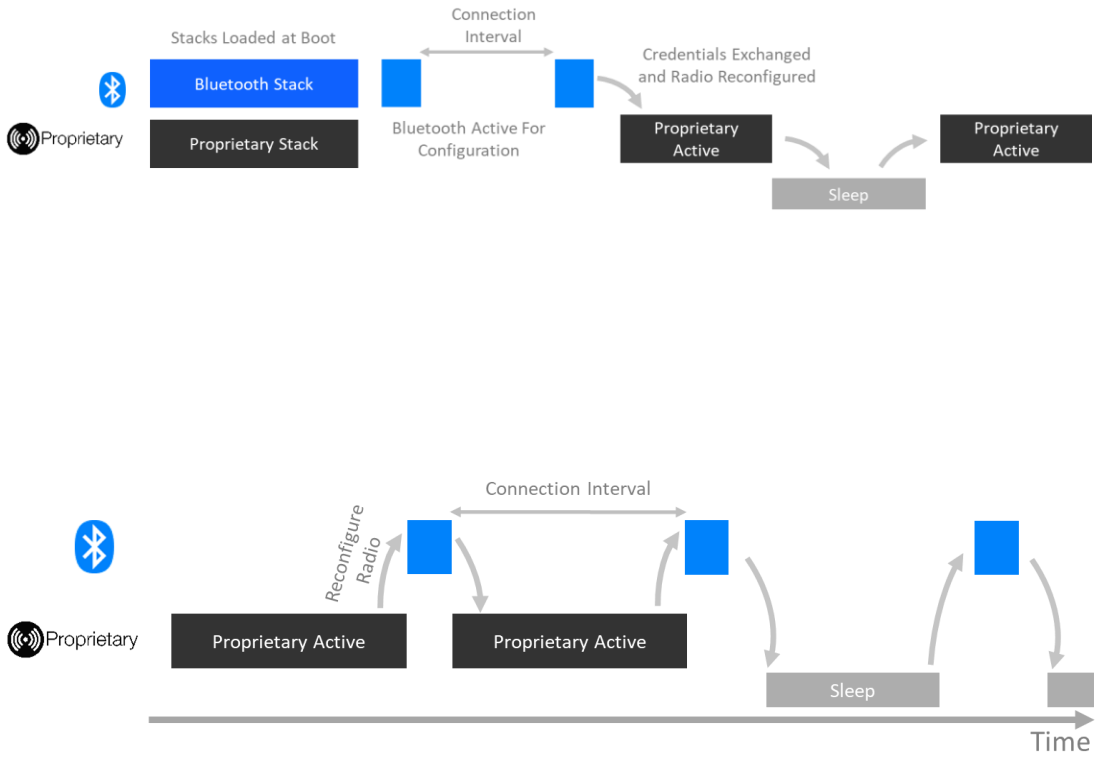
SoC approach can enable better protocol flexibility with simpler hardware design

- Can support many different protocols with single SoC family and compatible application code

Simplifies critical RF and protocol timing constraints with captive core architectures

- Offloads responsibility to dedicated processor cores for RF subsystem removing burden from application processor

Better Management of Complex RF Systems



Highly integrated wireless subsystem simplifies RF design

- Limits required external components and simplifies PCB design
- Lowers overall system cost by incorporating costly RF components

Radio abstraction commonizes interface allowing users to focus on application development

- Common API calls limit radio nuance when switching between protocols

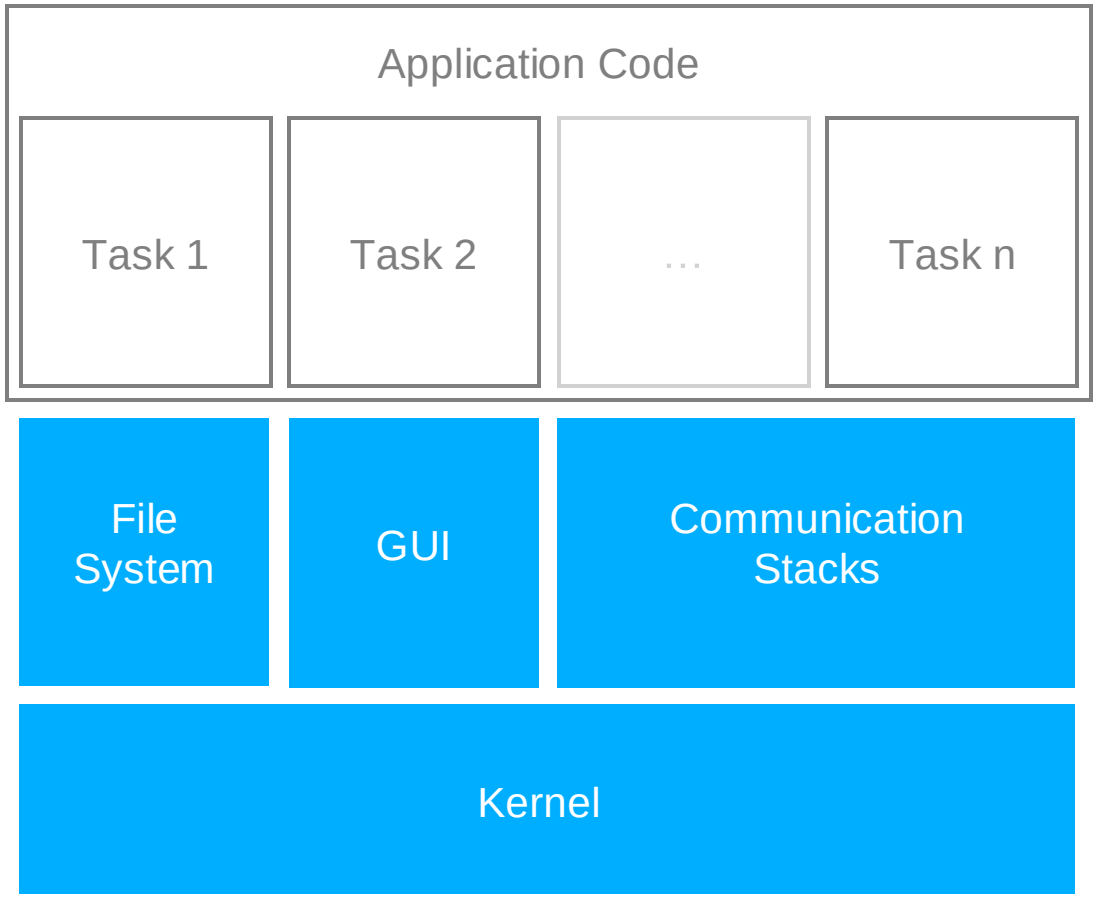
Dedicated sub-system core offloads critical radio functionality

- Ensures protocol timing is met while leaving application core resources available for developer use

Simplifies multi-protocol support with coexistence and timing managers

- Sub-system handles packet scheduling and manages network maintenance to limit potential issues

Growing RTOS Footprint



RTOS adoption is expanding rapidly

- More complex hardware solutions require more complex firmware architectures

Capabilities for RTOS options expanding as adoption increases

- Open RTOS offerings are becoming more inclusive and can be combined with other software components

Stacks, services, and Middleware can accelerate development time

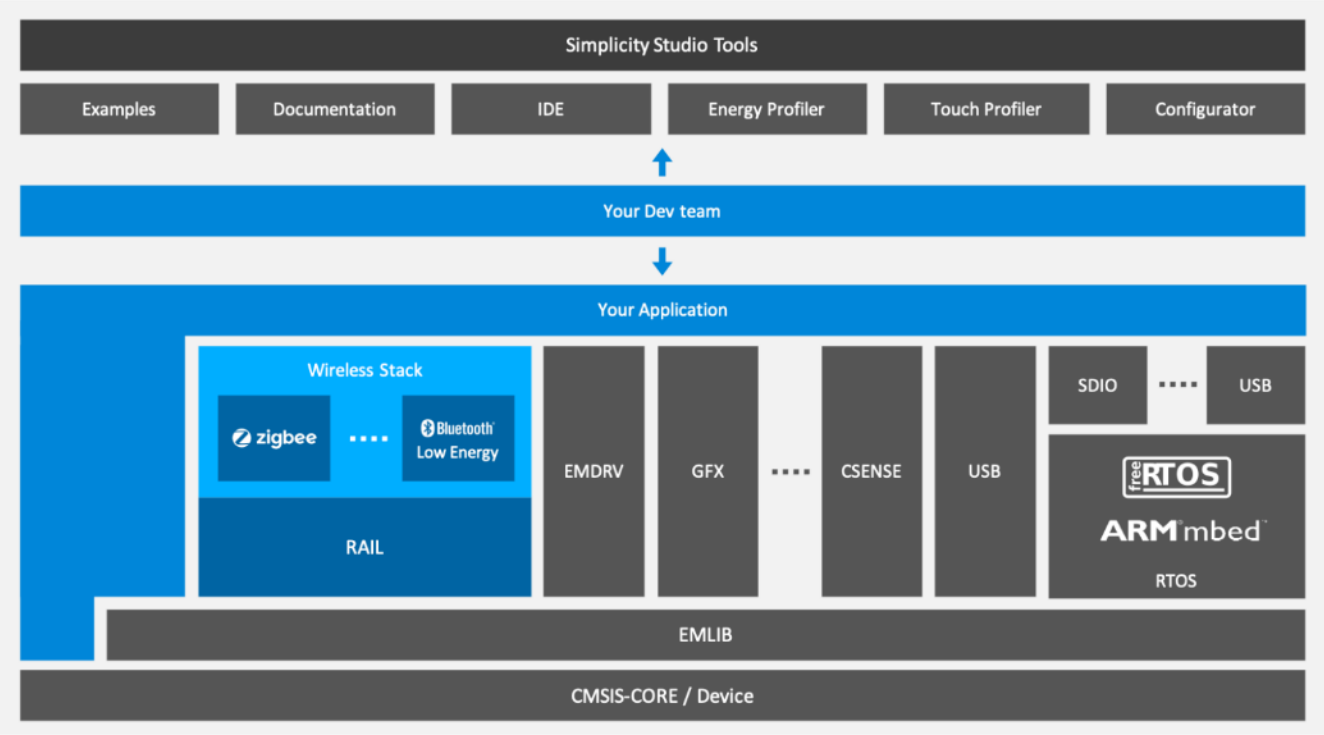
- Eliminates the need for developers to write thousands of lines of complex code

Hardware providers including more RTOS offerings with broader software platform

- Developers can more easily leverage full potential of hardware components

Simplifying Through Software

A Well Organized SDK



Simplicity Studio and Si SDK simplify application development

- Common tools and SDKs for entire product portfolio ease learning curve and improve reuse

Differentiated tools help with testing and development

- Energy Profiler and Network Profiler provide unique perspective for analyzing power and network performance

Firmware compatibility between connected and non-connected products simplifies end product development

- Simplifies code base management for multiple end product designs

EFM and EFR: A Common Solution for IoT Development

	BG	MG	FG	ZG	SG	PG
xG21	✓	✓				
xG22	✓	✓				✓
xG23			✓	✓	✓	✓
xG24	✓	✓				
xG25			✓			
xG26	✓	✓				✓
xG27	✓	✓				
xG28			✓	✓	✓	✓
	EFR Device Families					EFM

Multi-core architecture gives design flexibility and optimization across EFM and EFR platforms

- Dedicated application, radio[1], and security[2] cores share system burden for better resource utilization

Common development platform for connected and non-connected products

- Simplicity Studio gives developers a common development platform for entire product portfolio

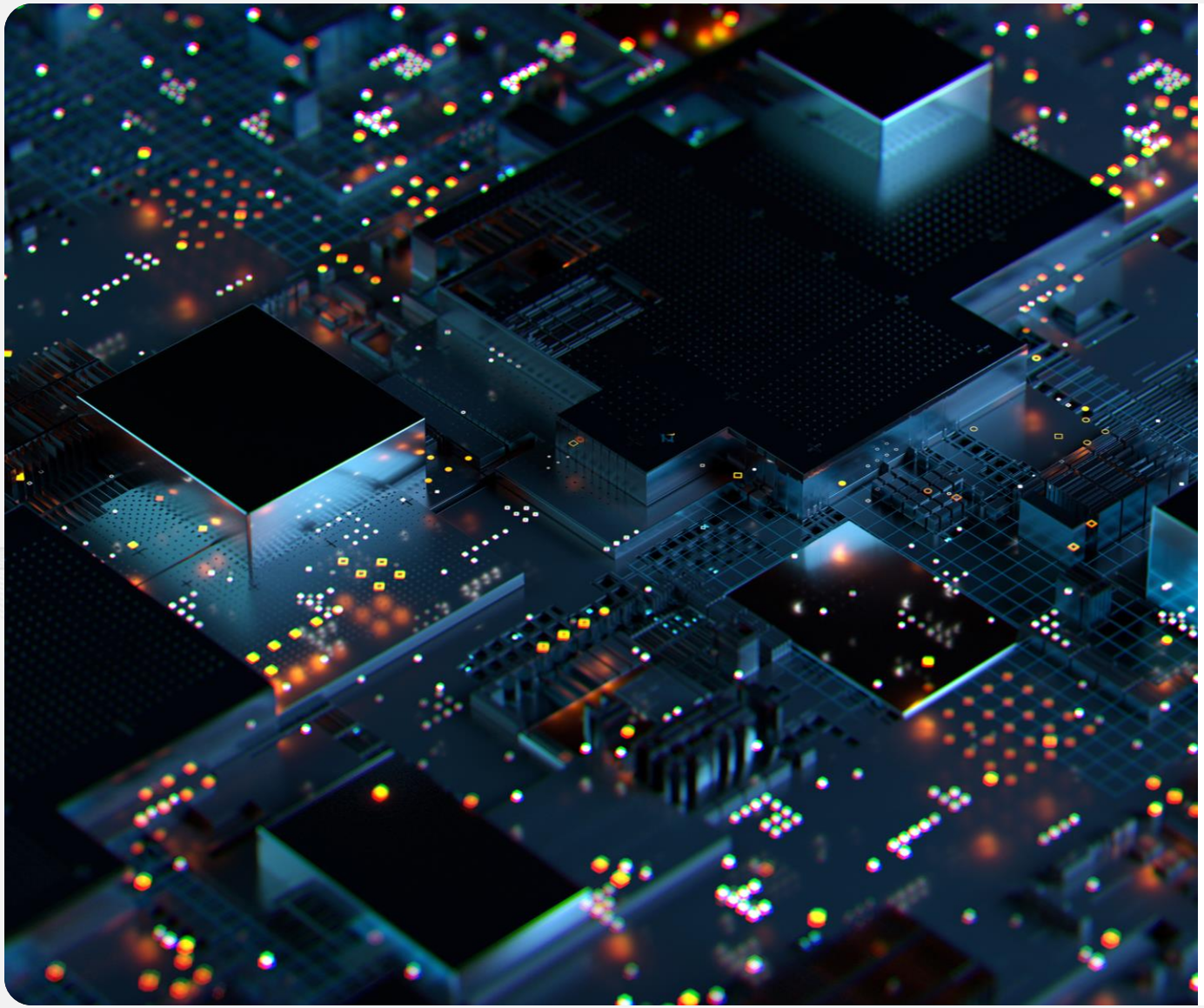
Common Security and AI/ML subsystems

- Allows for design consistency independent of connectivity needs

Footprint and firmware compatibility between EFM and EFR families

- Simplified SKU management and code base development lowers development cost and complexity

Evolving IoT Needs Reshaping MCU Architectures



Move to multi-core architectures improving power consumption and performance

- Distributed resources allow for system optimization more flexible power states
- Captive sub-system cores allow for better abstraction

RTOS footprint growing within MCU based products

- More complex architectures require better optimized firmware architectures
- Allows for platform portability and design flexibility

Chipset designs are becoming more specialized with more integration

- Application specific sub-systems drive more integration but may limit broad market fit
- Optimized MCU solutions lower overall system cost for targeted applications

Thank You