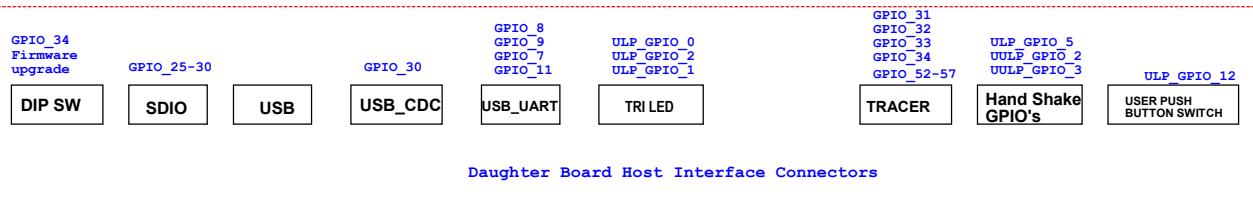
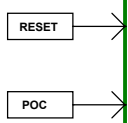
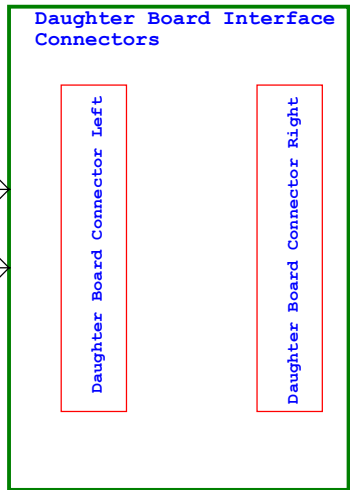
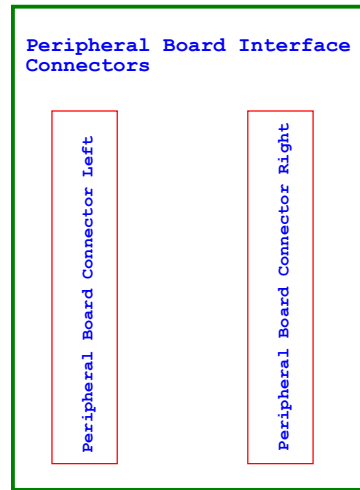


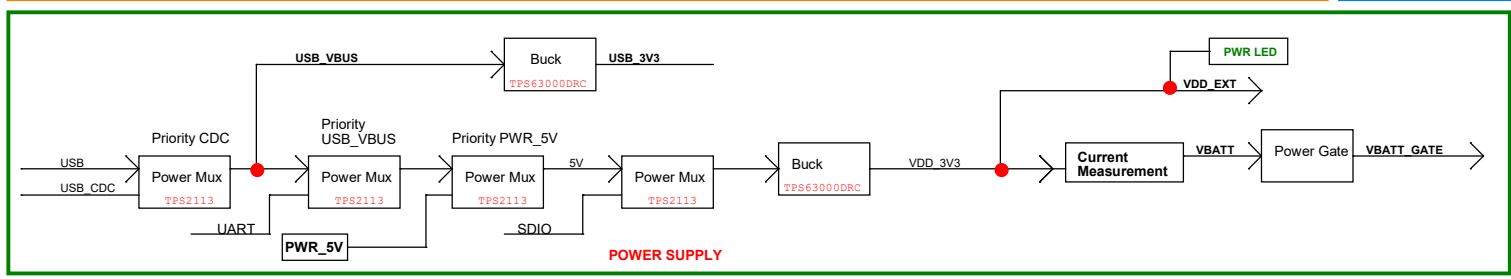
Base Board Block Diagram Rev1.4



Daughter Connector-Left side (J2)		Daughter Connector -Right Side (J3)	
ULP_GPIO_5	VDD_MOD	ULP_GPIO_15	GPIO_57
ULP_GPIO_4	GPIO_25	ULP_GPIO_14	GPIO_56
GPIO_10	ULP_GPIO_8	ULP_GPIO_13	GPIO_55
GPIO_12	ULP_GPIO_11	ULP_GPIO_12	GPIO_54
GPIO_15	ULP_GPIO_10	ULP_GPIO_3	GPIO_53
ULP_GPIO_6	UULF_GPIO_4	ULP_GPIO_2	GPIO_53
C_VDD	UULF_GPIO_1	GPIO_13	USB_VBUS
ULP_GPIO_0	GPIO_34	GPIO_14	USB_DM
ULP_GPIO_9	GPIO_33	MCU_RESET_N	USB_DP
ULP_GPIO_1	GPIO_32	GPIO_17	USB_ID
GPIO_29	GPIO_31	GPIO_18	USB_AVDD_1P1
GPIO_30	UULF_GPIO_3	GPIO_19	USB_AVDD_3P3
GPIO_28	UULF_GPIO_2	GPIO_39	GPIO_35
GPIO_11	UULF_GPIO_0	GPIO_21	GPIO_36
GPIO_8	VDD_3V3	GPIO_22	GPIO_37
GPIO_7	GPIO_46	GPIO_20	GPIO_38
GPIO_9	GPIO_47	GPIO_23	GPIO_42
GPIO_6	GPIO_48	GPIO_24	GPIO_43
ULP_GPIO_7	GPIO_49	GPIO_40	GPIO_44
GPIO_26	GPIO_50	GPIO_41	VDD_EXT
GPIO_27	GPIO_51	VDD_BB	GPIO_45
GPIO_2	VDD_5V	POC_IN	VOUTLDRF
VINMOD	GPIO_16	SDIO_18_33	

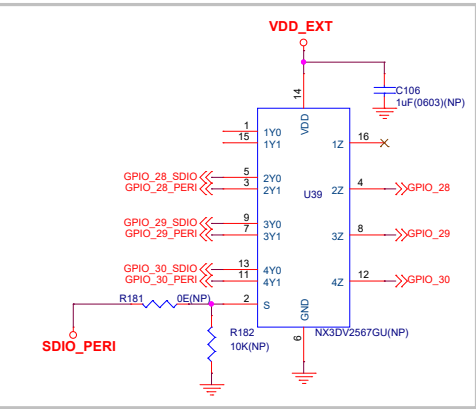
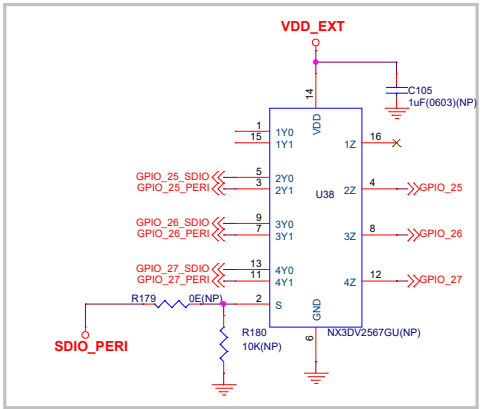
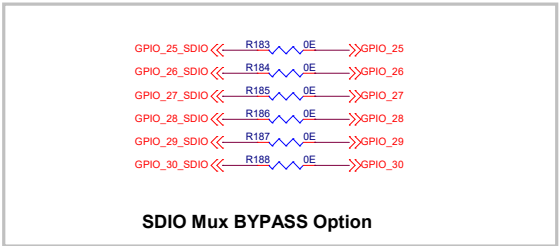
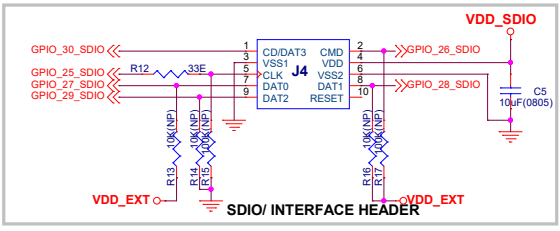
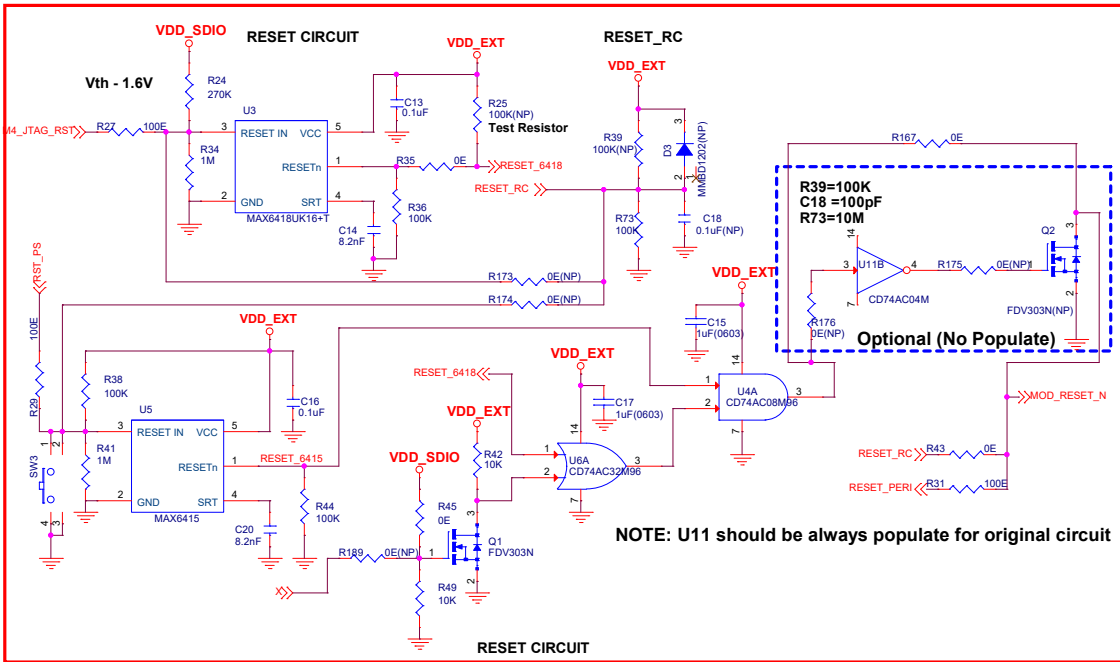
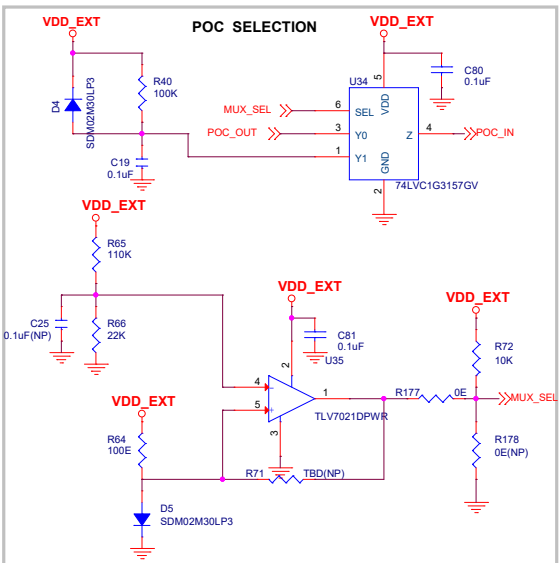
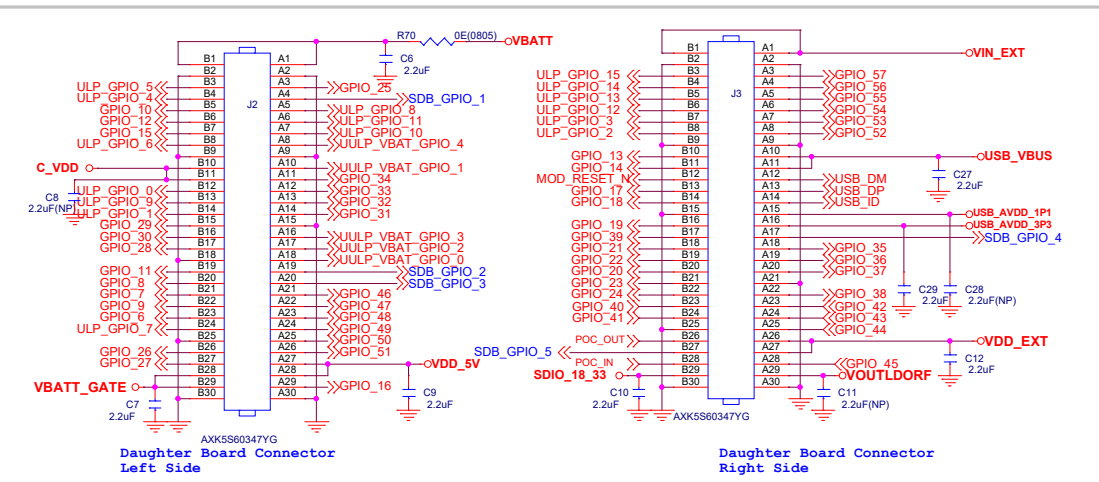


Peripheral Connector-Left Side (J2)		Peripheral Connector-Right Side (J3)	
GPIO_6	VDD_EXT	ULP_GPIO_3	UULF_GPIO_0
GPIO_7	GPIO_40	ULP_GPIO_4	UULF_GPIO_1
GPIO_8	GPIO_41	ULP_GPIO_5	UULF_GPIO_2
GPIO_9	GPIO_42	ULP_GPIO_6	UULF_GPIO_3
GPIO_10	GPIO_43	ULP_GPIO_7	UULF_GPIO_4
GPIO_11	GPIO_44	ULP_GPIO_8	
GPIO_12	GPIO_45	ULP_GPIO_9	
GPIO_13	GPIO_46	ULP_GPIO_10	
GPIO_14	GPIO_47	ULP_GPIO_11	VDD_5V
GPIO_15	GPIO_48	ULP_GPIO_13	DIE2_VOUTLDRF
GPIO_16	GPIO_49	ULP_GPIO_14	
GPIO_17	GPIO_50	ULP_GPIO_15	
GPIO_18	GPIO_51		
GPIO_19	GPIO_52		
GPIO_20	GPIO_53		
GPIO_21	GPIO_54		
GPIO_22	GPIO_55		
GPIO_23	GPIO_56		
GPIO_24	GPIO_57		
GPIO_25	VDD_5V		
GPIO_26	VOUTLDRF		
GPIO_27			
GPIO_28			
GPIO_29			



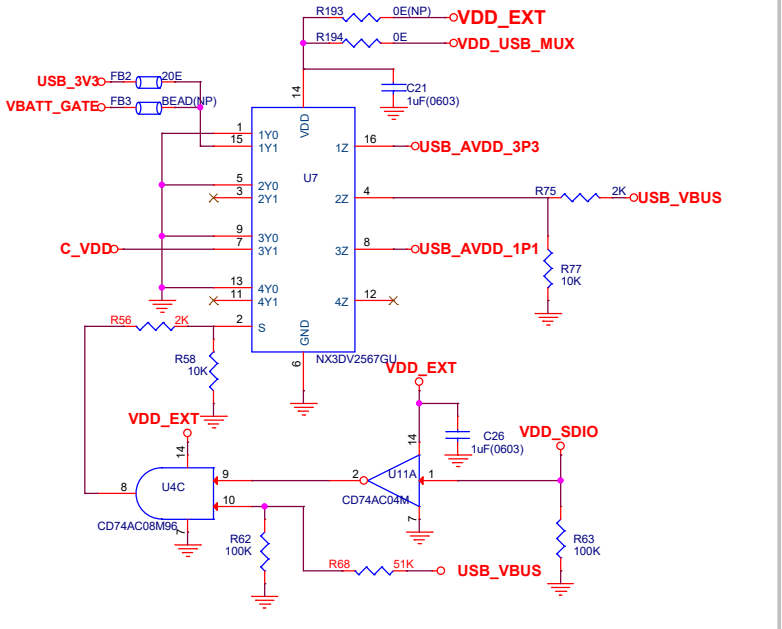
Silicon Labs Confidential

		400 W Cesar Chavez Austin, TX 78701	
Size	Title	RS9116-EVK-BASEBRD	
Part Number <Part Number>	Document Number Block Diagram	Rev 1.4	
Date:	Thursday, September 24, 2020	Sheet	1 of 6

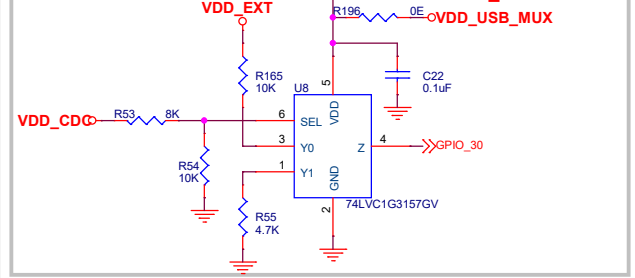


Silicon Labs Confidential

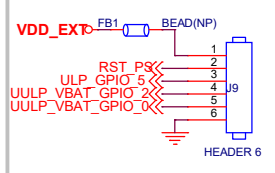
USB SUPPLY SELECTION



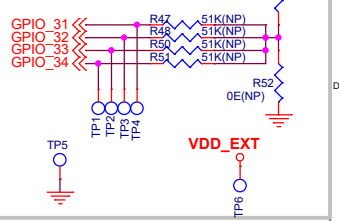
USB - CDC SELECTION



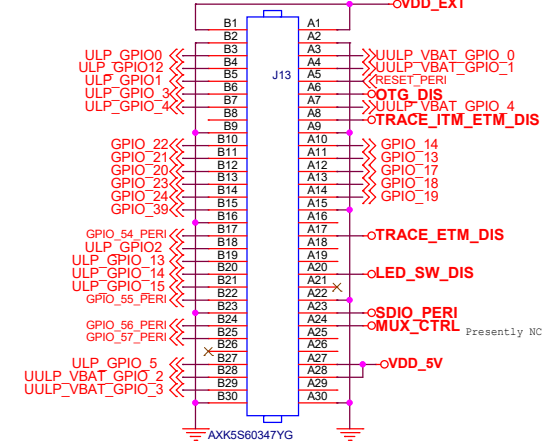
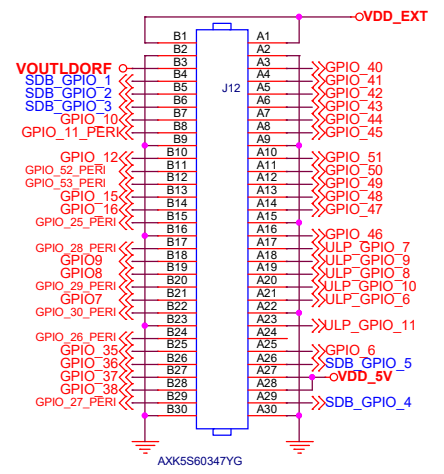
Power Save modes handshake



JTAG



Peripheral Board Connector

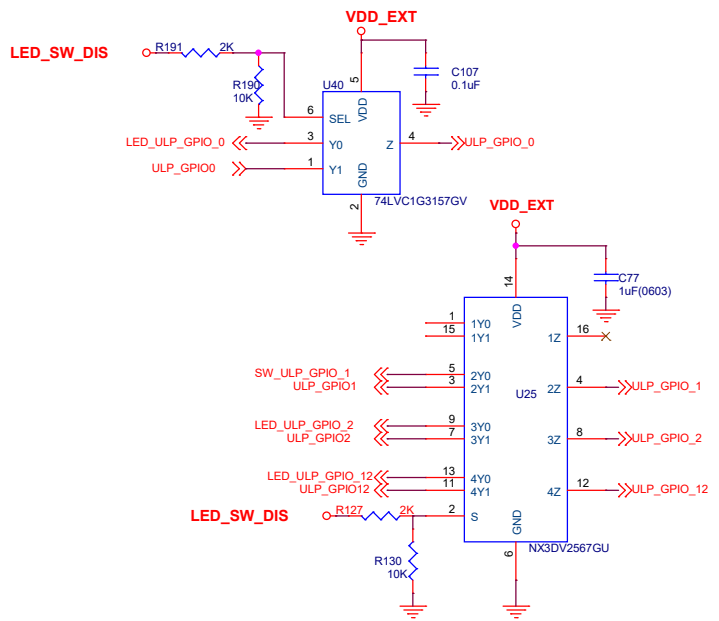


Peripheral Board Connector Left Side

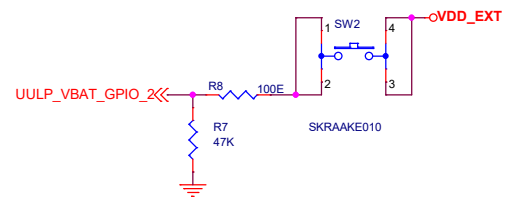
Peripheral Board Connector Right Side

Note: Ensure VCC On J13.A24 For SMTH Peripheral Card

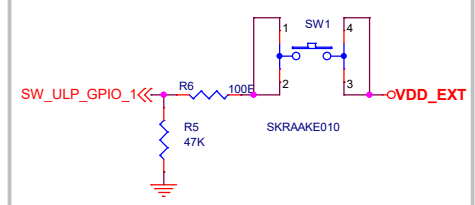
LED GPIO's MUX With Peripherals



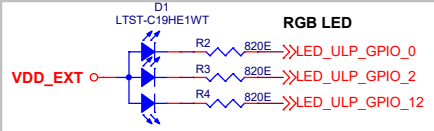
WAKE SWITCH



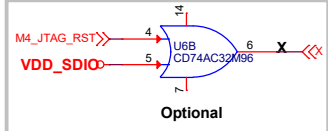
USER SWITCH

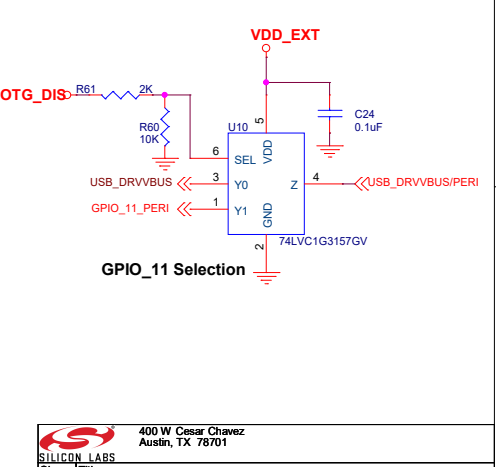
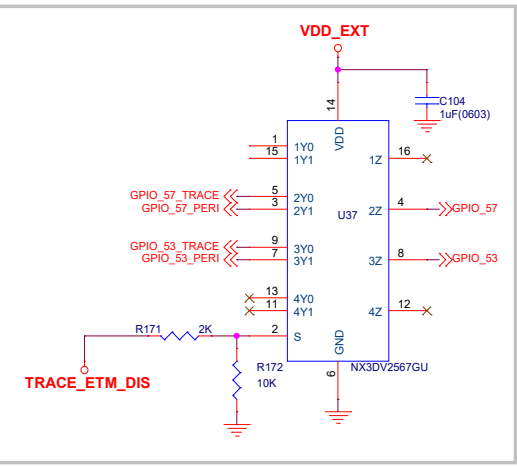
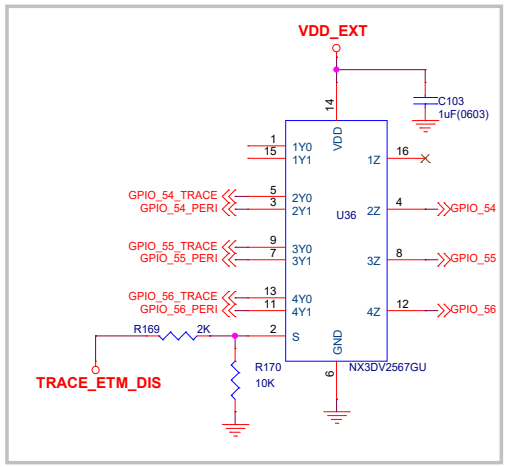
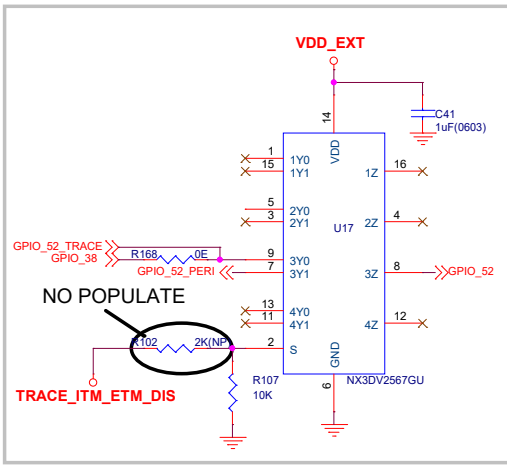
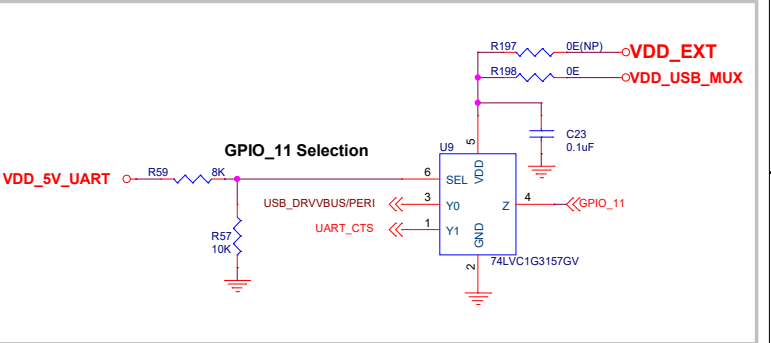
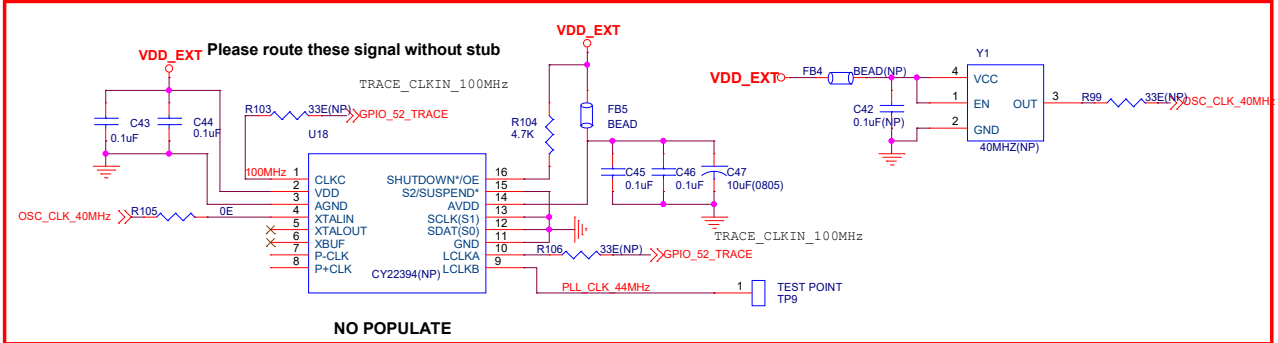
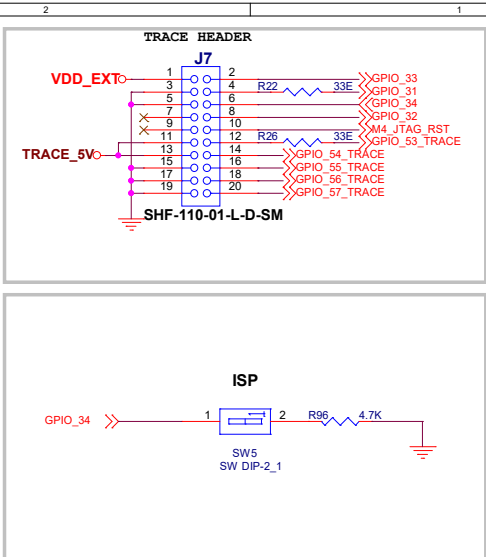
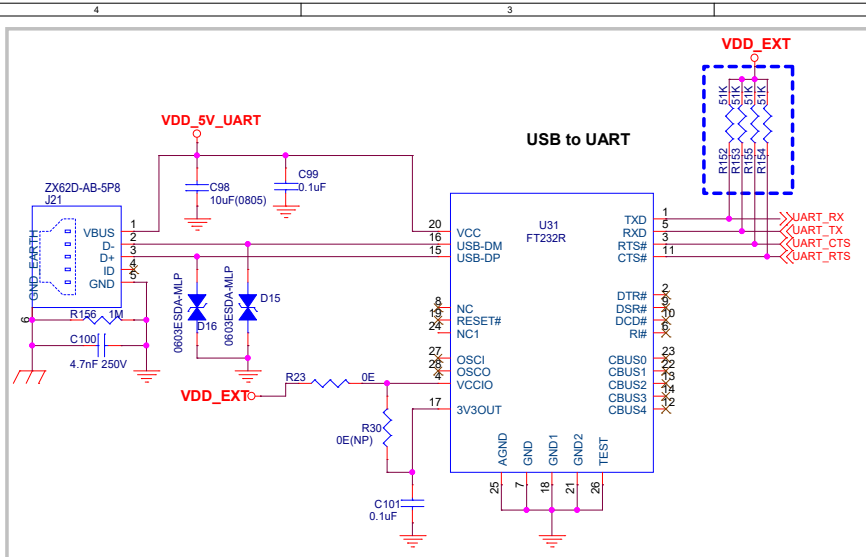
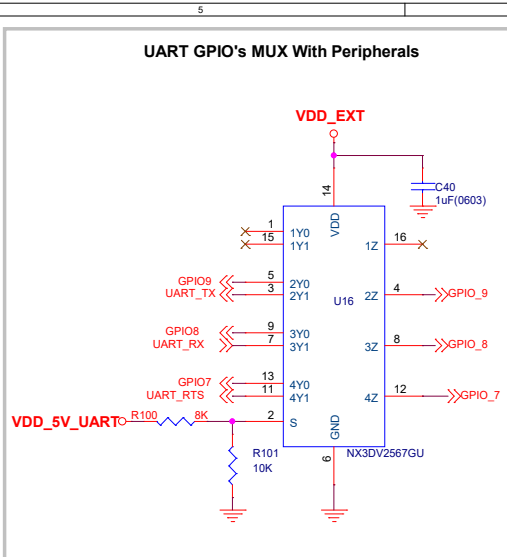


RGB LED



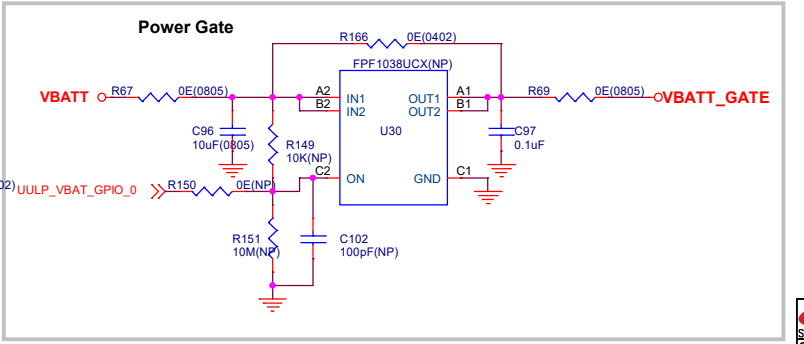
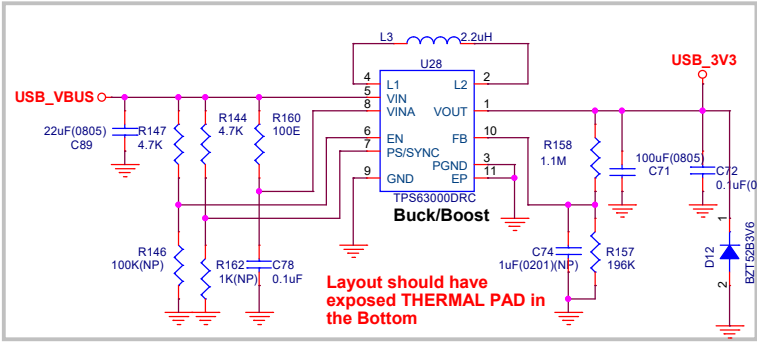
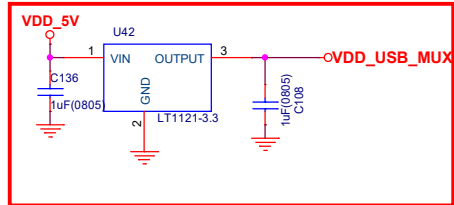
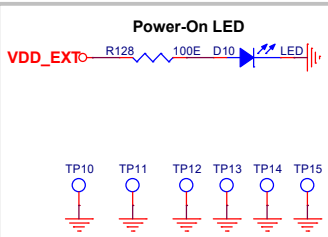
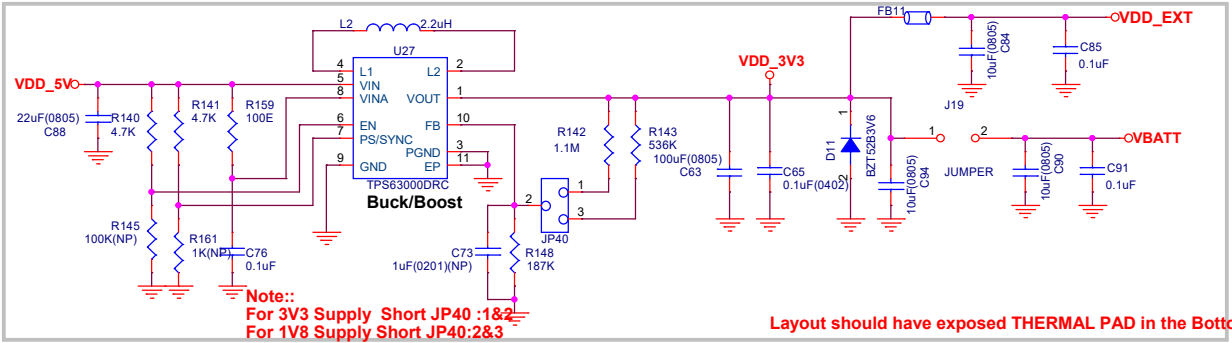
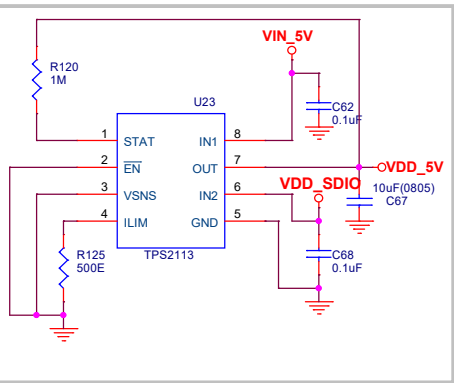
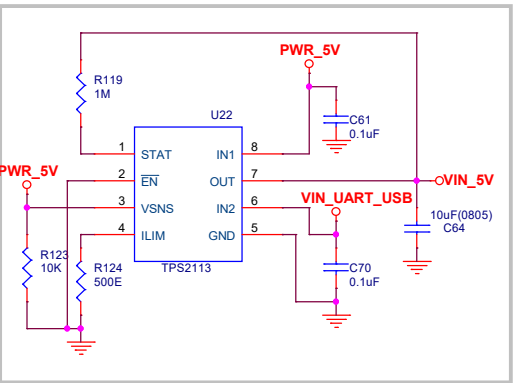
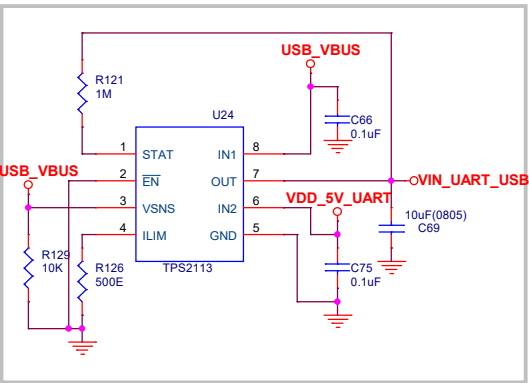
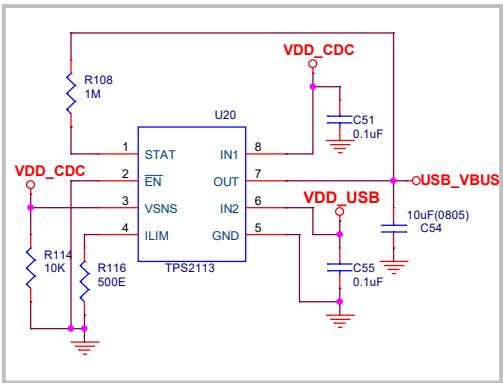
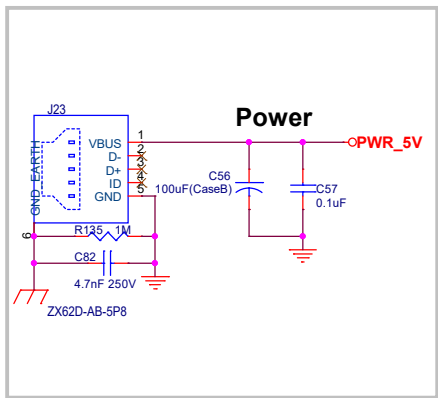
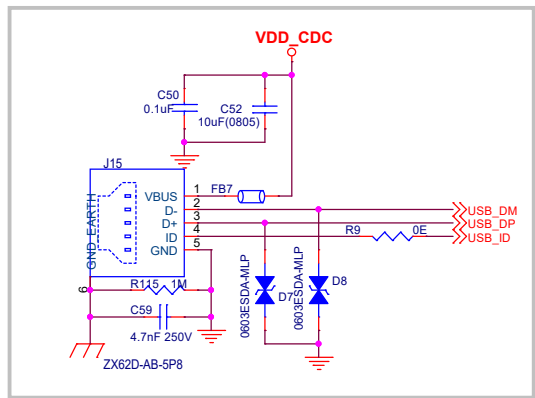
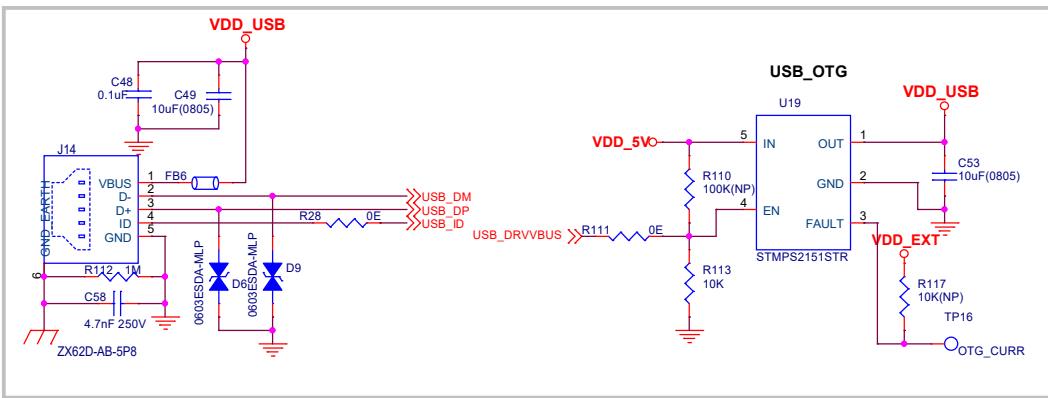
Optional





Silicon Labs Confidential

		400 W Cesar Chavez Austin, TX 78701	
Size	Title	RS9116-EVK-BASEBRD	
Part Number	Document Number	UART MUX	
<Part Number>		Date:	Thursday, September 24, 2020
		Sheet	4 of 6
		Rev	1.4



Revision Changes

Revision 1.4

To address silicon 1.4 related changes(24th Decemebr 2019)

- 1) In J9 connector UULP_VBAT_GPIO_3 changed to UULP_VBAT_GPIO_0
- 2) Added LDO LT1121-3.3 for generating VDD_USB_MUX
- 3) Option for VDD_USB_MUX & VDD_EXT provided for U7, U8, U9 supply pins
- 4) Title block changed from Redpine to Silabs on 24th September 2020

Revision 1.3

- 1) U16.1,U16.15,U16.16 pins changed to U16.9,U16.7,U16.8 respectively
- 2) USER SWITCH ULP_GPIO_12 changed to ULP_GPIO_1 & LED_ULP_GPIO_1 changed to ULP_GPIO_12
- 3) Optional circuit is added for reset signal @ 1.8V blackout monitor
- 4) Added MUX(U40) for LED0

Feature Changes

- 5) GPIO_38 is connected to U17 pin 1(@M7DB/M4SB Trace support)
- 6) Added MUXes(U36 &U37) on GPIO_54 to GPIO_57 and connected to Peripheral Headers
- 7) Moved GPIO_53 to MUX U37 from MUX U17(Trace Support for ITM_ETM)
- 8) Added MUXes(U38 &U39) on GPIO_25 to GPIO_30 and connected to Peripheral Headers along with bypass options
- 9) Added SDB_GPIO_1 - SDB_GPIO_5 to Daughter Board Headers and same has been brought to Peripheral Card Headers
- 10) Connected M4_JTAG_RST & RST_PS to RESET_RC(Optional Circuit: Added R173 & R174)

Name Changes

- 11) Changed the MUX U10 control name to OTG_DIS and connected to Peripheral Card Header

Revision 1.2

- 1) R39, D3,C18 made NOP, R43 Populated.
- 2) Added R73(100K) Pulldown on RESET_N
- 3) IC U8 input supply changed to VDD_EXT
- 4) Disconnected VDD_3V3 from J2 pin A19 & A20
- 5) R117 made NOP and Pull up supply changed to VDD_EXT
- 6) R100, R59, R53 changed to 8K
- 7) In USB Supply Section, added Beads FB2, FB3 on pin no of U7 (selection of USB_3V3(Default) and VBATT_GATE)
- 8) For U27 & U28 added decaps & Zener Diodes on output and RC network on VINA pin
- 9) Removed U21 and added U24
- 10) Removed U1 and added R163 &R164
- 11) Added decaps on all supplies in J2 & J3 Connectors
- 12) Changed Power Gate U30 to FPF1038UCX
- 13) Added Power Gate Bypass option
- 14) IC U8 Pin3 on one Pull up Resistor is added
- 15) C102 changed to 100pF


Revision 1.1

- 1) Added MUX in the GPIO_52 and GPIO_53 signals for SMIH WP& CD
- 2) RESET_N Connected to Handshake gpio header
- 3) Added R75 & R77 For USB_VBUS line
- 4) Added R72 & R73 For Comparator Feed back & Pull Up resistor
- 5) Added Buck/Boost for USB & USB CDC Power mux out connected
- 6) 1.8V Option for USB to UART converter
- 7) RESET_N Provision to Peripheral Connector

Revision 1.0

- 1) Initial Schematics

Silicon Labs Confidential

 400 W Cesar Chavez Austin, TX 78701		
Size	Title	
	RS9116-EVK-BASEBRD	
Part Number <Part Number>	Document Number Revision History	Rev 1.4
Date:	Thursday, September 24, 2020	Sheet 6 of 6