

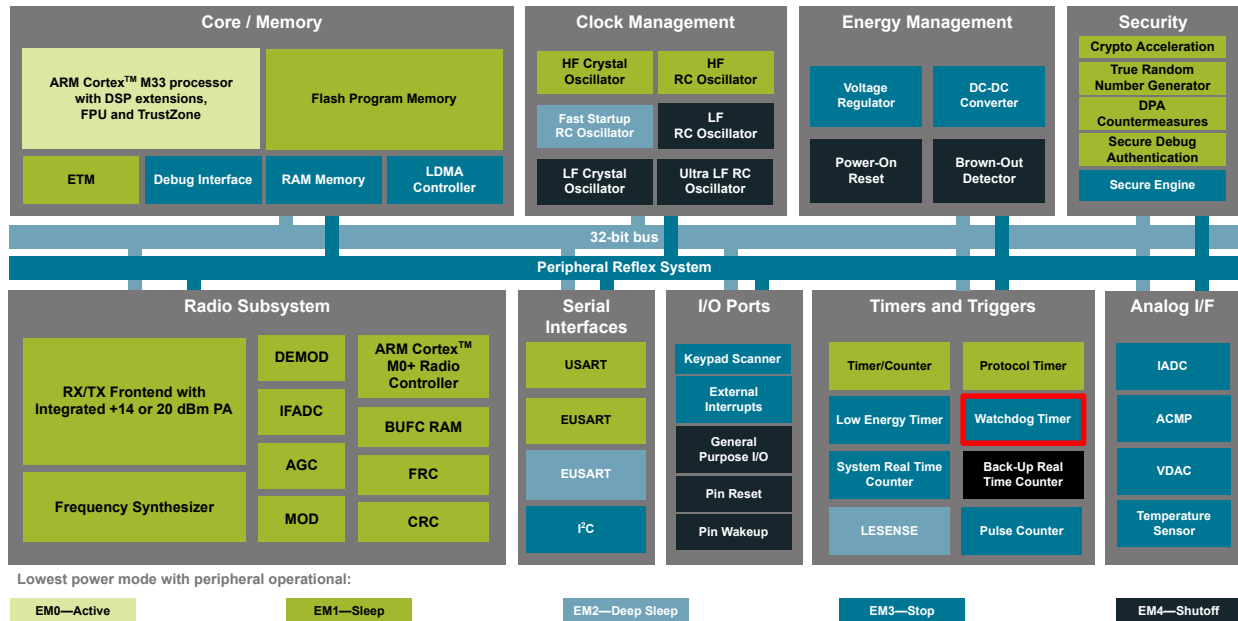
AN1426: Low-power "Lean Watchdog" Solution on EFR32 Series 2 Devices

This application note describes an alternative way to implement a watchdog functionality without using the built-in Watchdog of the EFR32 Series 2 devices.

Due to its location in a separate power domain, enabling the built-in Watchdog causes a high leakage current at elevated temperature, and the shown solution reduces this leakage current while retaining the watchdog functionality during EM2 sleep. In this application note, learn how to implement a low-power "Lean Watchdog" solution by combining BURTC and FAILDET peripherals on EFR32 Series 2 devices.

KEY POINTS

- Using a Watchdog in EM2 may add unnecessary current consumption on an EFR32FG23.
- Using BURTC and FAILDET as an alternative is possible.
- BURTC and FAILDET provide a similar protection level as native Watchdog.
- Alternative usage results in significant reduction of EM2 current.



1. What is a Watchdog?

In essence, a Watchdog is a digital hardware peripheral in a System-on-Chip (SoC) which is used to prevent software from stalling in an endless loop. The simplest Watchdog is nothing but a counter, which must be reset within a certain time period. If the reset does not happen, e.g., because of an endless software loop situation, the overflow event of the Watchdog counter will trigger a system reset.

The regularity of the Watchdog reset interval is adjustable and the clock source used as input for the Watchdog can be selected from various clock sources on the SoC. The reset interval and clock source for the Watchdog all depend on the requirements of the application.

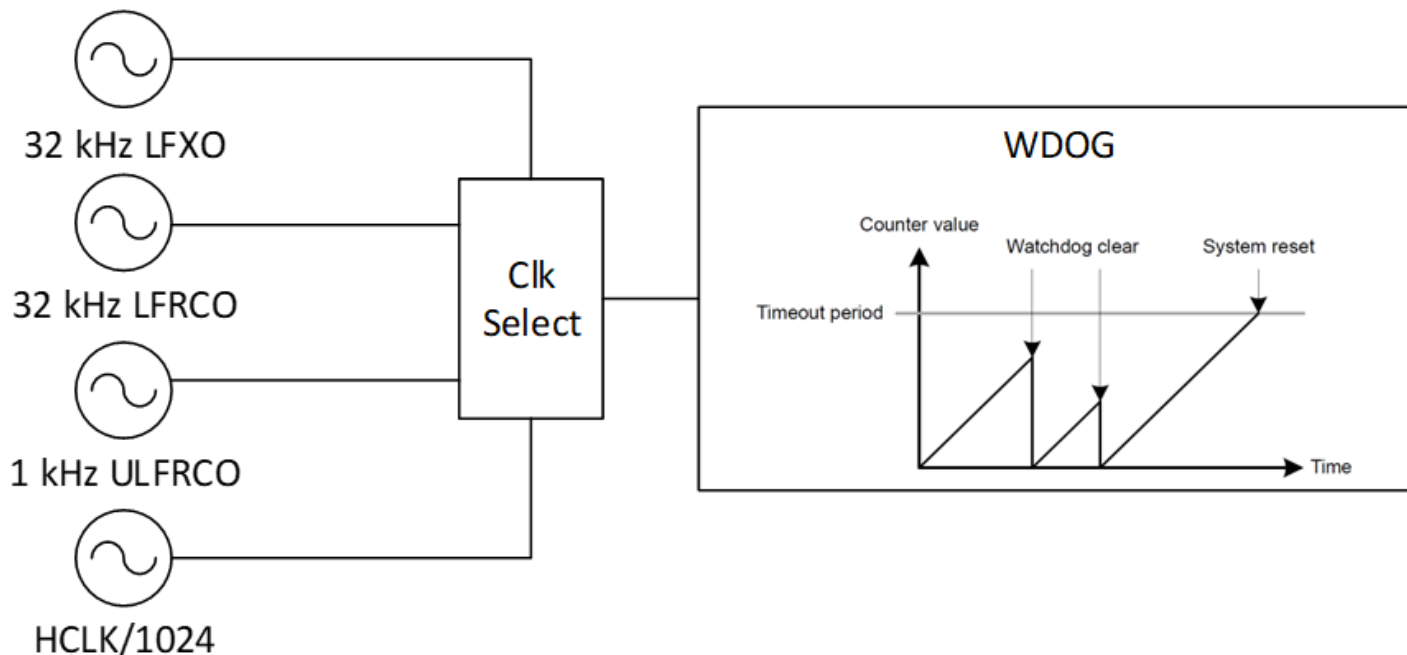


Figure 1.1. The Principle of a Watchdog

The reset interval for the Watchdog of an EFR32 Series 2 device is configurable from 9 up to 256000 Watchdog clock cycles, and depending on the selected clock source, this can be up to 256 seconds.

As shown in the figure above, the Watchdog is a counter that is incremented at a rate depending on the selected clock source. If the Watchdog is cleared, the counter is set to 0 and the counting starts over again. However, if the Watchdog is *NOT* cleared, the Watchdog will trigger a HW reset, and this will force all program counters to be reset and the software will start over again. It is important to note that the HW reset is triggered independently, of any software intervention, interrupt priority or other software related interventions.

If the Watchdog triggers a HW reset, the occurrence of this event is stored in a register which can be read by the software upon restart and a proper action on the Watchdog reset event can be taken if required by the application. The register storing the reset reason is called `EMU_RSTCAUSE`.

For more information on how the EFR32 Series 2 Watchdog works, refer to the application note, [AN0015.2: EFR32 Series 2 Watchdog](#).

2. Watchdog Current Consumption

The power supply structure of an advanced SoC, like the EFR32 Series 2 devices, is divided into multiple power domains. This structure enables management of the current consumption during sleep modes; if a feature is not required, there is no reason to allow its power domain and waste energy.

The implementation of power domains of EFR32 Series 2 devices are very similar, although with minor differences. Refer to the data sheets of the individual devices for detailed descriptions.

For an EFR32xG23 device, the power domains are structured as follows:

Table 2.1. EFR32xG23 SoC Power Domains

| Always on in EM2/EM3 | | Selectively on in EM2/EM3 | | | |
|----------------------|--------|---------------------------|-----------|--------------|---------|
| PDHV | PD0A | PD0B | PD0C | PD0D | PD0E |
| <u>LFXO</u> | SYSRTC | LETIMER0 | HFRCOEM23 | DEBUG | GPIO |
| <u>BURTC</u> | FSRCO | IADC0 | HFXO | <u>WDOG0</u> | KEYSCAN |
| LFRCO | LCD | PCNT0 | | <u>WDOG1</u> | PRS |
| ULFRCO | | ACMP0 | | EUSART0 | |
| | | ACMP1 | | I2C0 | |
| | | LESENSE | | | |
| | | VDAC0 | | | |

The two power domains PDHV and PD0A are always powered, and PDHV is even available during EM4 shutoff mode, which is the lowest possible power state of an EFR32 Series 2 device.

If the application requires usage of a Watchdog, the power domain PD0D must be enabled in order to use the Watchdog, and it is the enabling of the PD0D power domain that will increase the current consumption of the SoC when in EM2/EM3 mode. The implementation of the Watchdog itself does not contribute much to the current consumption, approximately 200 nA, but since it is inside the power domain PD0D, which must be enabled, the net current consumption is significantly higher.

On the other hand, if the application requires usage of any other peripherals located in the PD0D power domain, e.g., for serial communication during EM2/EM3, where the EUSART0 must be enabled to support this requirement, then PD0D must be enabled in order to use the EUSART. The additional current of the Watchdog is negligible since PD0D is already enabled due to the additional feature required.

To summarize this aspect of the power domains:

- If the only reason for enabling the PD0D power domain is to support usage of the Watchdog and if EM2 leakage current is a concern, the method for implementing a Lean Watchdog described in this application note can be a solution.
- If any other peripherals located in the PD0D are required by the application, enabling the Watchdog does not contribute with any significant current consumption on top of the current consumption of the power domain itself.

The graph below shows how enabling the PD0D power domain and the Watchdog will result in an increased current consumption across temperature when compared to an application where the PD0D is disabled:

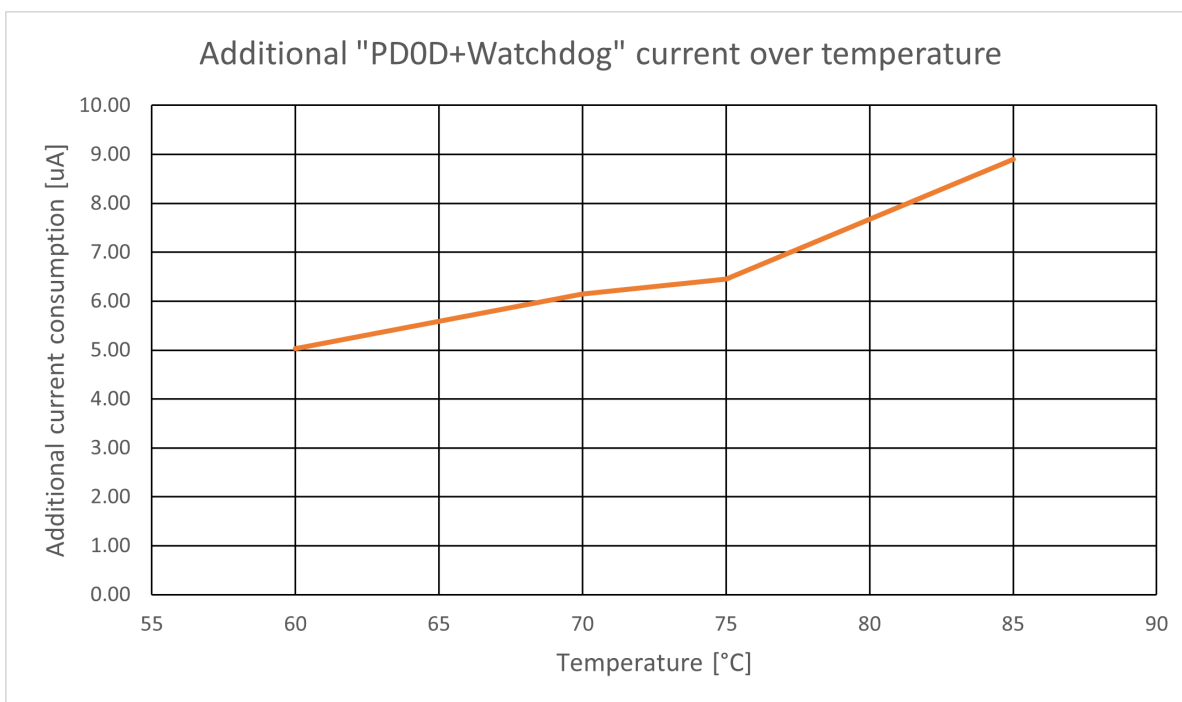


Figure 2.1. Additional Leakage Current of the PD0D Power Domain + Enabled Watchdog Measured Across Temperature. Measured on an EFR32FG23 Device

Note: The results shown in the figure above were measured on a small set of EFR32FG23s, and these were the results that we saw on our set. Although customers can expect to see additional current consumption on this order of μA , the exact amount of current will vary between each chip due to process variations.

The Lean Watchdog solution presented in the next sections will cut down this current consumption by more than a factor of 20 while still providing protection against endless software loops.

3. An Alternative Solution: The Lean Watchdog

The built-in Watchdog provides protection against the following situations:

1. Prevents software from an endless loop in EM0.
2. Prevents the device from endless EM2 sleep.
3. Provides a HW reset if the Watchdog is not reset at a regular interval smaller than the timeout period of the Watchdog.

An alternative to the built-in Watchdog should at least provide the same level of protection against malfunction in situations #2 and #3, but at a lower current consumption. Situation #1 can always be covered by the built-in Watchdog.

3.1 The Back-Up RTC

EFR32 Series 2 devices have a timer called the Back-Up Real Time Clock (BURTC). As shown in [Table 2.1 EFR32xG23 SoC Power Domains on page 3](#), this timer is in the always powered power domain, meaning that using the BURTC does not increase the power down current as when enabling the PD0D power domain used by the built-in Watchdog.

The Back-Up RTC has multiple clock sources.

1. LFXO: Low-frequency 32.768 kHz crystal oscillator
2. LFRCO: Low-frequency 32.768 kHz internal RC oscillator
3. ULFRCO: Ultra-low-frequency 1 kHz internal RC oscillator

Just like the built-in Watchdog, the BURTC is a timer which counts up from 0. When it reaches a pre-defined count value, the timer will overflow, which can result in an EM2 wakeup via an interrupt.

If the BURTC is configured to a timeout period larger than the EM2 sleep period and the device does **not** wake up from the EM2, the BURTC will awake the device from EM2 and the software can handle the failure or reset the device.

So, in summary, the BURTC method:

- counts during EM2, and
- awakes the device from EM2 in case firmware wrongly configured the EM2 sleep time

without causing a leakage current situation as the one shown in [Figure 2.1 Additional Leakage Current of the PD0D Power Domain + Enabled Watchdog Measured Across Temperature. Measured on an EFR32FG23 Device on page 4](#).

3.2 The FAILDET Feature

For a timed wake-up from a sleep mode, the SoC requires a low-power clock source. EFR32 Series 2 devices offer three different clock sources which can be used as sleep clock sources:

1. LFXO: Low-frequency 32.768 kHz crystal oscillator
2. LFRCO: Low-frequency 32.768 kHz internal RC oscillator
3. ULFRCO: Ultra-low-frequency 1 kHz internal RC oscillator

For high accuracy applications, where the duration of the sleep period matters, the LFXO is the sleep clock source to select.

If the LFXO malfunctions or is tampered with during EM2, the device may be prevented from exiting EM2, which will result in an endless EM2 sleep.

To prevent this situation, the EFR32 Series 2 devices have a built-in monitor of the LFXO clock source. If the oscillator or crystal stops or does not output a clock pulse when expected, a failure interrupt can be raised. The failure occurs if fewer than three LFXO clock positive edges happen during one 1 ms. The failure interrupt is called FAILDET.

FAILDET can be configured to awake the device from EM2, and the software can act accordingly on the unexpected EM2 wakeup.

Because the FAILDET is part of the LFXO, according to [Table 2.1 EFR32xG23 SoC Power Domains on page 3](#), using this feature does not require enabling an additional power domain since the LFXO is in a power domain which is always powered.

So, in summary, the FAILDET:

- Monitors a stable EM2 power down clock source.
- Monitors if the EM2 power down clock source is stopped.
- Can be configured to awake the device from EM2 if unstable or no clock is detected.

All of the above can be accomplished without causing a leakage current situation as the one shown in [Figure 2.1 Additional Leakage Current of the PD0D Power Domain + Enabled Watchdog Measured Across Temperature. Measured on an EFR32FG23 Device on page 4](#).

4. Combining the FAILDET and the BURTC to a "Lean Watchdog" Solution

If the two methods described (FAILDET and BURTC) are combined and used together, a functionality just like the built-in Watchdog can be obtained:

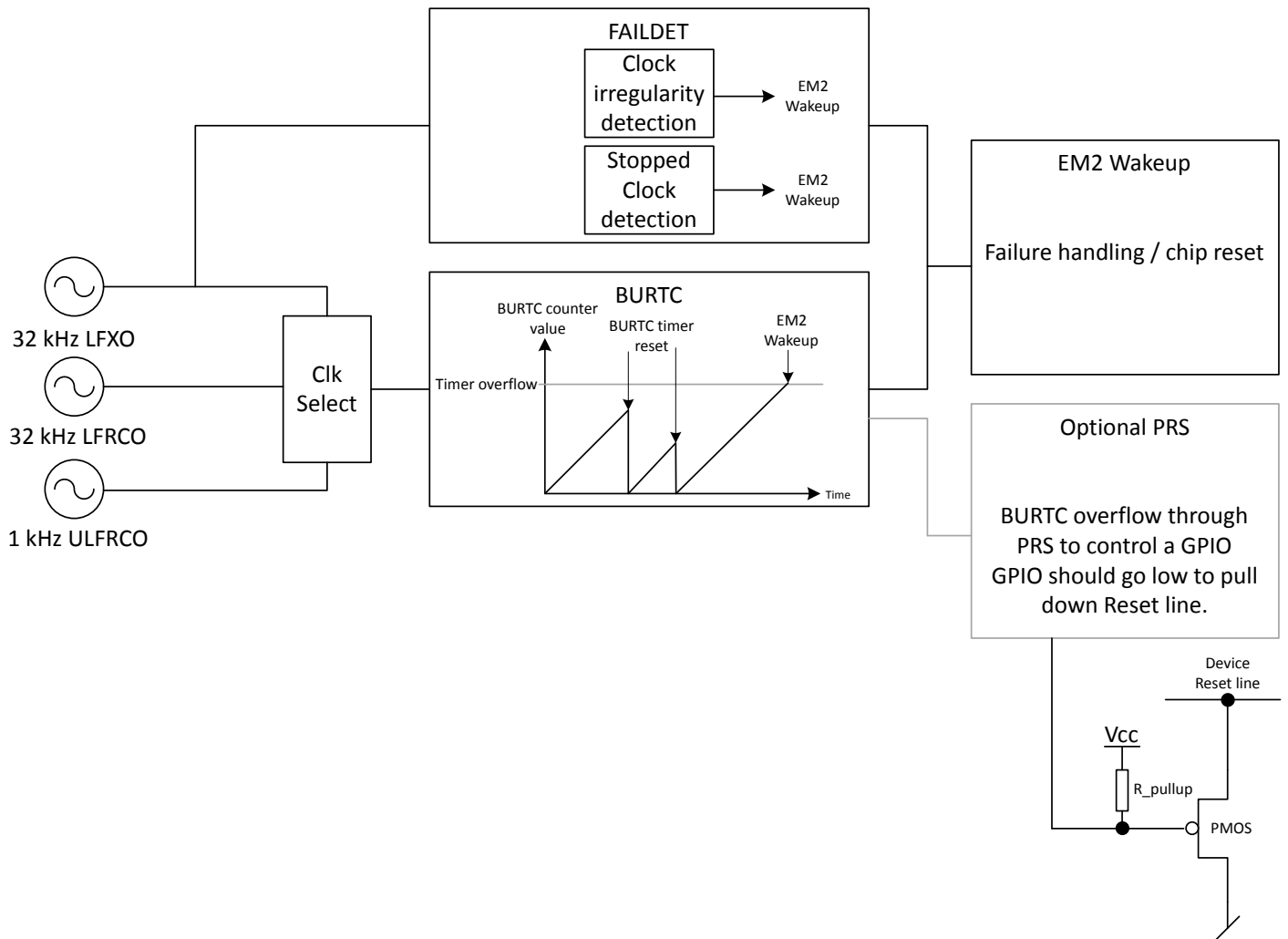


Figure 4.1. FAILDET and BURTC Combined to a Lean Watchdog Solution

Using the FAILDET to monitor the LFXO during EM2 ensures that the SoC always wakes up in case of a missing or unstable LFXO clock. Combined with the BURTC overflow event, which will happen if the part does not exit EM2, this solution provides the same functionality as the built-in Watchdog without the need to enable an additional power domain.

An optional functionality is depicted in the figure above, Optional Peripheral Reflex System (PRS). The PRS of an EFR32 Series 2 device makes it possible to create logic connections (AND, OR, NOT, etc..) between internal signals and the General Purpose Input Output interface (GPIO interface). Here the PRS system can be used to connect the overflow event of the BURTC timer with a GPIO pin. This GPIO pin can then (when using a couple of simple devices like a resistor and a PMOS transistor) be connected to the hardware reset pin of the device. An overflow of the BURTC due to missing intervention from the software can now trigger a true hardware reset.

Below is a comparison of the two "watchdog" functionality solutions:

Table 4.1. Comparison of Built-in Watchdog and the Lean Watchdog Method

| Built-in Watchdog | Lean Watchdog using FAILDET and BURTC |
|---|--|
| Prevents software from endless loops in EM0 | Built-in Watchdog: Prevents software from endless loops in EM0 |
| Prevents device from endless EM2 sleep | BURTC: Prevents device from endless EM2 sleep |
| | FAILDET: Prevents unstable LFXO clock during EM2 sleep |
| Hardware reset if Watchdog is not reset | Software triggered chip reset by BURTC / FAILDET |
| Must enable additional power domain | All functionality covered by an always powered power domain |
| Automatically triggers a hardware reset when overflowed | BURTC: Triggers a software interrupt |

As shown in the table above, the Lean Watchdog has two advantages: It provides additional protection against unstable LFXO clock during EM2 sleep and can be implemented without enabling additional power domains.

5. Leakage Current Comparison

The previous section describes how to implement Lean Watchdog as an alternative solution to the built-in Watchdog. The reason for using such an alternative solution is to prevent an increase in EM2 leakage current when power domain of the built-in Watchdog is enabled.

Below is a graph depicting two current lines over temperature: The blue line shows the actual measured additional current consumption of the suggested Lean Watchdog method, whereas the orange line shows the additional current consumption of the built-in Watchdog when the power domain PD0D is enabled:

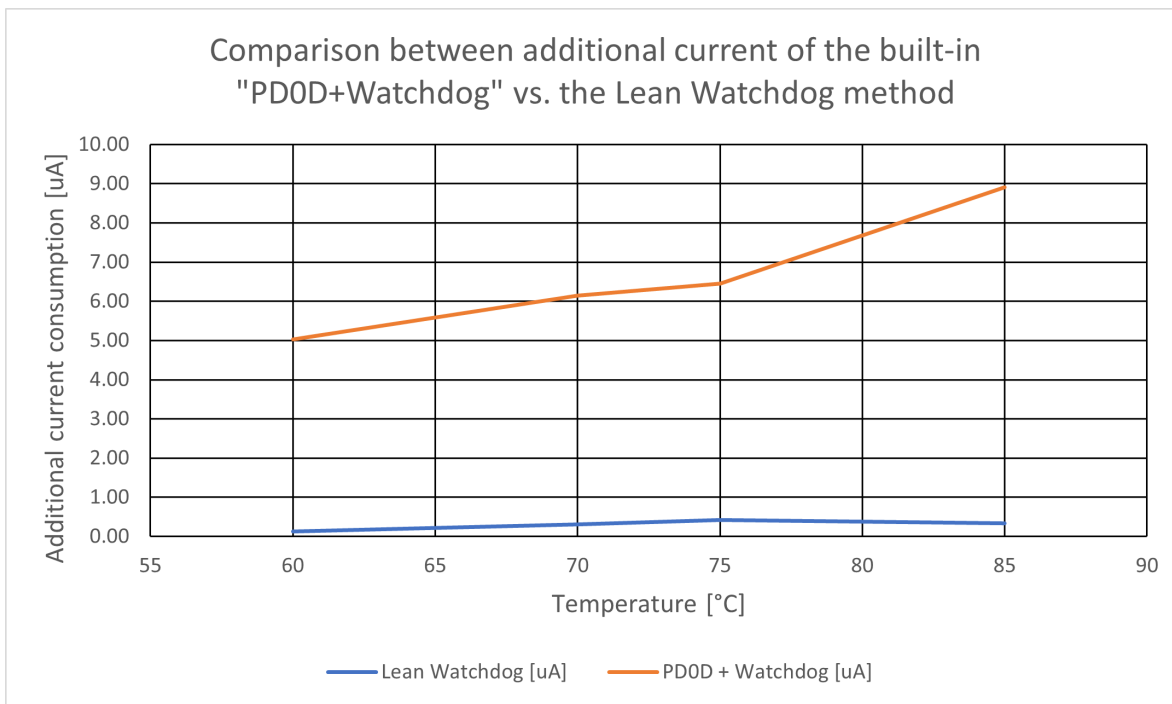


Figure 5.1. Additional Current Consumption of Built-in Watchdog in Power Domain PD0D vs. Lean Watchdog, Measured on an EFR32FG23 Device

Note: The results shown in the figure above were measured on a small set of EFR32FG23s, and these were the results that we saw on our set. Although customers can expect to see additional current consumption on this order of μA , the exact amount of current will vary between each chip due to process variations.

As shown in the figure above, using the Lean Watchdog method with PD0D powered down consumes a significantly less amount of current than using the built-in Watchdog with PD0D powered on.

6. Considerations

If the application to build:

- requires usage of a Watchdog functionality,
- is sensitive to EM2 current consumption, or
- does not need other peripherals from the power domain PD0D,

then using the Lean Watchdog method should be considered as an alternative solution because of lower current consumption and a comparable protection functionality against malfunction during EM2 sleep.

However, the built-in Watchdog triggers a **HW** reset if not reset in a timely manner, whereas the Lean Watchdog triggers **an interrupt** if not reset in a timely manner.

This implies that the interrupts from the BURTC and FAILDET must be configured to have the highest priority of all interrupts used in the application, so that **if** a situation arises where one of the interrupts is triggered, the interrupt routine **will** be called and a software triggered reset can be released from within the interrupt routine for the device to start over.

On the other hand, because the reset must be triggered by an interrupt handling routine, this also enables the possibility of having error handling prior to the reset event and perhaps prevent a reset. When using the built-in Watchdog, the hardware reset is triggered by the built-in Watchdog and the reason for the reset can be analyzed **after** the event. With the Lean Watchdog, the reason for a reset can be analyzed in the interrupt handling routine, and if required, the part can be reset using a software triggered reset. If the code implemented in the interrupt handling routine can handle the erroneous situation, a reset can be saved, and the device can re-enter EM2 or enter EM0 without having to reset.

7. Solution Availability

An implementation of the Lean Watchdog example can be found in the Silicon Labs Platform Applications Example Github repository: https://github.com/SiliconLabs/platform_applications/tree/master/platform_lean_watchdog.

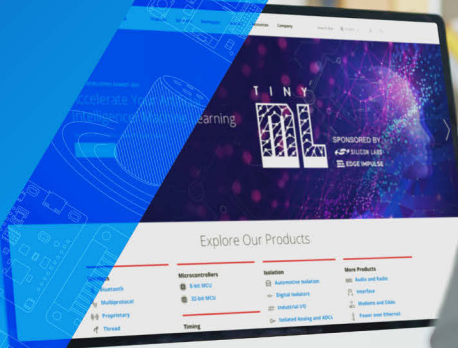
8. Revision History

Revision 1.0

September 2023

- Initial version

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