AN1439: SiWx917 Hardware Debugging Guidelines

This document provides guidelines for debugging hardware-related issues with SiWx917. Users may encounter issues while working with SiWx917-based prototypes or products. Most of these issues are simple to resolve and may require only minor fixes. Users can resolve the issues by following this set of guidelines.

KEY POINTS

- General Debugging Guidelines
- Issue-specific Debugging Guidelines

Table of Contents

1. Introduction

This document covers procedures to resolve issues that SIWx917 users commonly encounter. It contains a few general guidelines that must be followed irrespective of the issue. The guidelines have been divided based on the severity of the issue encountered by the user, for cases when no prototype/product board is working and when a few of them are not working.

There are general guidelines and issue-specific guidelines in this document. The general guidelines must be followed before proceeding with the issue-specific guidelines.

The guidelines are common for both SiWG917(SoC) and SiWN917(NCP) OPNs unless explicitly mentioned.

2. Debugging Test Points

This section contains information about pins that are useful for debugging.

2.1 SoC Debugging Options

#	Interface	Pins	Notes
1	JTAG	JTAG_TMS_SWDIO (A16) JTAG_TDO_SWO (B15) JTAG_TDI (B16) JTAG_TCK_SWCLK (A17)	JTAG is an industry standard protocol used for debugging and boundary testing. It is based on a standard given by IEEE.
2	Serial Wire Debug (SWD)	SWD Interface: JTAG_TMS_SWDIO (A16) JTAG_TCK_SWCLK (A17) SWV Interface: JTAG_TDO_SWO (B15)	SWD is an ARM specific protocol designed specifically for micro debugging. Additionally, users can implement Serial Wire Viewer (SWV) mode, in which one-bit serial protocol is used and this reduces the number of output signal to one. When combining SWV with SWD, the TDO pin normally used for JTAG protocol can be shared with SWV. This can be done using JTAG_TDO_SWO pin
3	ETM Trace	DEBUG_TRACECLK (sourced via MCU_CLK_OUT) DEBUG_TRACED0 DEBUG_TRACED1 DEBUG_TRACED2 DEBUG_TRACED3	ETM provides high bandwidth instruction trace via four dedicated traces. The MCU_CLK_OUT frequency must be in the range of 40MHz to 90MHz to Instruction trace using ETM component. GPIO 53:57 are recommended for ETM trace but GPIO 46:51 can also be used. If external Flash and external PSRAM are connected on GPIO 46:51 and GPIO 52:57, then ETM Trace cannot be used.
4	In-System Programming (ISP)	UART: Si917_GPIO_8 (A36) Si917_GPIO_9 (A24) SPI: Si917_GPIO_25 (B40) Si917_GPIO_26 (A1) Si917_GPIO_27 (B39) Si917_GPIO_28 (A44) SDIO: Si917_GPIO_25 (B40) Si917_GPIO_26 (A1) Si917_GPIO_27 (B39) Si917_GPIO_28 (A44) Si917_GPIO_29 (A43) Si917_GPIO_30 (A42)	ISP can be used for programming or reprogramming the flash through boot loader using UART/SPI/SDIO. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to gain the control and to reprogram the flash. Connect JTAG_TDO_SWO to ground while using ISP.
5.	Serial Logs	UART2_TX or ULP_UART_TX	This pin will output the serial debug logs for the ThreadArch (TA) processor.

2.2 NCP Debugging Options

#	Interface	Pins	Notes
1.	Host Interfaces	UART: Si917_GPIO_8 (A36) Si917_GPIO_9 (A24) SPI: Si917_GPIO_25 (B40) Si917_GPIO_26 (A1) Si917_GPIO_27 (B39) Si917_GPIO_28 (A44)	User can utilize the host interface to send commands to the chip for testing and debugging. If a particular host interface does not work, user can connect a different host interface and debug the chip.
2.	Serial Logs	UART2_TX or ULP_UART_TX	This pin will output the serial debug logs for the ThreadArch (TA) processor.

3. General Debugging Guidelines

Follow these guidelines before proceeding to issue-specific guidelines.

3.1 No Boards Working

The following are debugging guidelines:

1. Ensure that the design is per the latest documents (especially the data sheet) available on the website.
2. Measure all Output Voltages of the IC, and ensure they are generated per specifications.
3. Capture the power sequence waveform in detail (Power supply inputs, POC_IN, RESET_N). Ensure the following:
    a. Signals are meeting timing requirements as per the data sheet.
    b. There is no unintentional second reset after power-up.
4. Check if the chip is getting reset due to an external event like a dip in supply or voltage overload. Ensure there are no software interrupts or loops that might be leading to incorrect resets.
5. Noise is within 50mVpp for these signals.
6. Power supply input voltages are within the operating conditions mentioned in the data sheet.
7. Ensure that there are no soldering/assembly issues. Analyze X-ray images and ensure there are no power and ground shorts.
8. Swap the ICs between working Silicon Labs evaluation boards and failing boards and check the functionality of both.
9. Ensure the issue is not due to environment, by using different PCs, instruments, and debug probes.
10. If the product application seems to have the issue, run example applications from Silicon Labs to ensure the general functionality of the chip is as expected.
11. If an external clock is used, disconnect that, and use the internally generated 32kHz clock through software configuration.
12. Check the working of the 40MHz external crystal by probing it using an oscilloscope with active probe having low capacitance(<1pF) and high bandwidth.
13. For SoC products, ensure that the external memory devices are working and firmware and(or) application code are programmed correctly.
14. Probe the power supply traces with reverse polarity in diode mode of the multimeter and compare the voltage values with a working Silicon Labs evaluation board.
15. Check the MAC IDs and lot code information of the modules/SoCs and share with Silicon Labs. Check the package specifications in the datasheet for more information.

3.2 Few Boards Working

The following are debugging guidelines:

1. Ensure the design is per the latest documents (especially the data sheet) available on the website.
2. Ensure Schematics and Layout are followed per the latest data sheet.
3. Swap the modules/SoCs between working and failing boards and check the functionality.
4. Ensure that there are no soldering/assembly issues. Analyze X-ray images and ensure there are no power and ground shorts.
5. If the product application seems to have the issue, run example applications from Silicon Labs to ensure the general functionality of the chip is as expected.
6. For SoC products, ensure that the external memory devices are working and firmware and(or) application code are programmed correctly.
7. Check the working of the 40MHz external crystal by probing it using an oscilloscope with active probe having low capacitance(<1pF) and high bandwidth.
8. Probe the power supply traces with reverse polarity in diode mode of the multimeter and compare the voltage values with a known good board.
9. Check the MAC IDs and lot code information of the modules/SoCs and share with Silicon Labs. Check the package specifications in the datasheet for more information.

4. Issue-Specific Debugging Guidelines

A few issues might require additional debugging. Follow the general guidelines and then proceed with the subsequent guidelines.

4.1 Host Interface Issues

The module is unable to communicate with the host in NCP/SoC mode. The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Run with a lower clock speed for SPI/SDIO host interfaces; reduce the baud rate for the UART interface and check the functionality.
3. If multiple host interfaces are used, firstly ensure that only one host interface is used after power up and tristate the other host interface. Disconnect one of the interfaces from the module and test the working of the boards.
4. Increase the power up sequence time interval between VBATT and POC_IN to 100 ms and the time interval between POC_IN and RESET to 100 ms and check that the board is working.

4.2 Low Output Tx Power

The Tx power numbers are not meeting data sheet specifications. The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure that the software configurations are correct.
3. Try using a higher cap (like 4.7 uF, 10 uF, etc.) value on the PA2G_AVDD pin and other power amplifier pins available.
4. Try adding a lower cap (like 0.1 uF, 10 pF, etc.) value on the PA2G_AVDD pin and other power amplifier pins available.
5. Check for any noise on board, as some noise may interfere with the power supply or RF area.
6. Ensure the RF frequency variation is within 25 ppm (IEEE standard).
7. Account for any losses in the RF path from the chip to the antenna/connector.
8. Ensure the DC blocking capacitors and other LC components are as per the reference schematics in the data sheet.
9. Ensure that the tuning circuitry matches the antenna used.
10. Measure the conducted RF power near a test point placed before the antenna. To measure conducted RF power (in Spectrum Analyzer), ensure the RF wiring on-board is done appropriately, and remove tuning circuitry and antenna from the RF path. If the conducted RF power is as expected, the issue could be due to tuning circuitry or the antenna itself.
11. Measure the conducted RF power on the SiWx917 chip pin by placing pigtail connector on it, and check if the performance is as per the data sheet specifications. If this conducted RF power is as expected, the issue could be due to front-end circuitry (switch, filter, etc.).

4.3 Poor Connectivity with Access Point

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Follow guidelines given in Section 4.2.
3. Check sniffer captures to identify Tx/Rx issues.
4. As recommended, add an 8.2 pF DC blocking cap on the RF path.
5. Ensure that the tuning circuitry matches the antenna used.
6. Check the Tx powers and Rx sensitivity in PER mode and compare the values with the data sheet.

4.4 Access Point (AP)/Station Mode-Related Issues

- AP Mode: AP Discovery Issues
- Station Mode: Joining/Scanning issues

The following are the debugging guidelines for this issue:

- Ensure all the above general debugging guidelines are followed.
- Follow guidelines given in Section 4.2.
- Ensure there are no soldering or assembly issues on your board, and ensure the chip is soldered as per the recommendations.

4.5 Module Overheating Issue

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure there are no soldering or assembly issues on your board, and ensure the chip is soldered as per the recommendations.
3. Lower the throughput of the module and check the working. Sometimes, higher throughput may cause heating issues.
4. Check the current consumption and ensure the values are within the ones mentioned in the data sheet.
5. Check the Tx powers and Rx sensitivity in PER mode and compare the values with the data sheet.
6. Ensure all GPIOs are configured correctly. Incorrectly terminated GPIOs can lead to overall high current consumption and heating. Sometimes these issues cannot be reproduced as it may be related to environmental factors as well.
7. Ensure there is no physical damage on the chip or any soldering and assembly issues.

4.6 Module Not Working at Extreme Temperatures

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure parts used on board along with SiWx917 are rated for the operating temperature.
3. Ensure the environment temperature is within the specifications of the particular OPN.
4. Lower the throughput of the module and check that it's working. Sometimes, higher throughput may cause issues.

4.7 High Current Consumption

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure all input signals work at the same voltage level as their IO supply domain. For example, the RESET_N signal should be at 3.3 V only if UULP_VBATT_2 is connected to 3.3 V.
3. Ensure the chip does not consume higher current due to physical damage. This can be checked by measuring the current using the example applications provided by Silicon Labs and comparing with the values mentioned in the data sheet.
4. Ensure all GPIOs are configured correctly. Incorrectly terminated GPIOs can consume current and lead overall high current consumption. Sometimes, these issues cannot be reproduced as it may be related to environmental factors as well.
5. Ensure all systems connected to the chip are not powered if the chip is not powered. Parasitic power through the I/O pins can also damage the internal subsystems of the chip.

4.8 SiWG917 SoC – External Memory Access Issues

- Change in memory locations or data.
- Application on the external memory location does not load.

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure the memory devices used on board with SiWG917 are as per our recommendations.
3. Ensure that noise in the powers supply is not impacting the memory devices during read/write cycles.
4. Ensure there are no unintentional resets while programming/reading/writing to the memory device.
5. Ensure frequency specifications are met during programming/reading/writing to the memory device.
6. Lower the frequency of memory clock and check the working of the memory.
7. Ensure there are no timing issues for the interface used.

4.9 Sensor/Actuator/Peripheral Issues

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure that the software configurations are correct.
3. Ensure the GPIO configuration is correct according to the GPIO Multiplexing table.
4. Ensure GPIO is not damaged by ESD or other environmental factors, check the working of the external device with another GPIO.
5. Ensure the peripheral and the GPIO voltage supply domains are correctly matched.
6. Ensure there are no timing issues for the interface used.

4.10 DAC/ADC Issues

The following are the debugging guidelines for this issue:

1. Ensure all the above general debugging guidelines are followed.
2. Ensure that load on the pin is not causing the issues by disconnecting it and checking the output of the DAC.
3. Ensure the software configuration of the DAC/ADC programmed correctly.
4. Ensure there are no timing issues for the interface used.

5. References

- Application Notes
- Data Sheets
- Schematics and Design files

Smart. Connected. Energy-Friendly.

IoT Portfolio
www.silabs.com/products

Quality
www.silabs.com/quality

Support & Community
www.silabs.com/community

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com