AN1448: SiWx917 Power Supply Architecture and Configurations

This application note describes hardware design considerations for SiWx917 devices. Topics covered are power supply configuration, external supplies, power sequencing, and decoupling.

For radio-related hardware guidelines, refer to AN1423: SiWx917 RF Matching and Layout Design Guide.

KEY POINTS

- SiWx917 multiple power supply configurations
- Summary of power levels and converters
- Bypassing of internal power converters
- Power sequencing diagram
- Importance of decoupling capacitors and star-routing

1. Device Compatibility

- SiWG917
- SiWT917
- SiWN917

2. Power Supply Overview

The SiWx917 is a flexible, ultra-low power wireless device with multiple configuration options regarding power supplies. Existing on-board power supplies can be used, bypassing the internal ones of the IC, to easily integrate the device. This flexibility opens multiple budget saving alternatives when creating a design. In the following section, these options will be discussed.

2.1 Supply Voltages

The IC utilizes multiple voltage levels to be energy-friendly, using the lowest sufficient voltage where it can. These voltage levels can be divided into two categories: external and internal. The user must provide external levels; the various internal regulators and converters of the IC create internal ones.

Note: For absolute maximum rating, refer to the SiWG917 data sheet.

External Levels:

- 3.3 V
- 1.8 V

Internal Levels:

- 1.8 V
- 1.45 V
- 1.15 V
- 1.05 V
- 0.75 V

Only external levels must be provided by the user, so two scenarios of connecting on-board power sources are possible:

- **3.3 V single supply**: All systems can be supplied from this voltage
- **3.3 V and 1.8 V supply**: All systems can be supplied from 1.8 V, except the PA2G_AVDD pin that requires 3.3 V

Note: When the dual supply configuration is used, if the radio is not transmitting, PA2G_AVDD can be left floating/pulled down.

2.2 Power Converters Summary

The following table contains all the power converters that create the internal voltage levels from the external ones. It lists every converter that is in the PMU subsystem (discussed later) and the ULP regulators subsystem. The latter one is responsible for supplying the Cortex-M4 core in even the lowest consumption sleep mode, so it cannot be bypassed or left floating.

Table 2.1. Power Converters Summary

Subsystem	Power Input Pin	Input Voltage	Output Voltage	Max. Load	Power Output Pin	Supplies	Converter	Max. Efficiency[1]
PMU	VINBCKDC	1.8 V/3.3 V	1.45 V[2]	250 mA	VOUTBCKDC	RF and digital blocks	LC DC-DC (Switching converter)	88%
	VINLDOSOC	1.45 V	1.15 V	200 mA	VOUTLDOSOC	Digital blocks	SoC LDO (Linear regulator)	73%
	VINLDO1P8	1.8 V/3.3 V	1.8 V	48 mA	VOUTLDO1P8	Internal (or Eternal) Flash	Flash LDO (Linear regulator)	53%[3]
	RF_AVDD1&2&3	1.45 V	1.15 V	20 mA	VOUTLDOAFE	RF and AFE	LDO RF&AFE (Linear regulator)	79%
ULP Regulators	ULP_VBATT_1&2	1.8 V/3.3 V	1.05 V	—	UULP_VOUTSCDC_RETN	Always-ON core logic and low power peripherals	SC DC-DC (Switching converter)	57%
	—		0.75 V	—		Only low power Always-ON core logic	LDO075 (Linear regulator)	70%

Note:

1. At maximum load current.
2. The output voltage is after the inductor, not at the output pin.
3. At 3.3 V input voltage.

2.3 Power Management Unit

Most internal voltages are controlled by the Power Management Unit (PMU), which can operate in different modes.

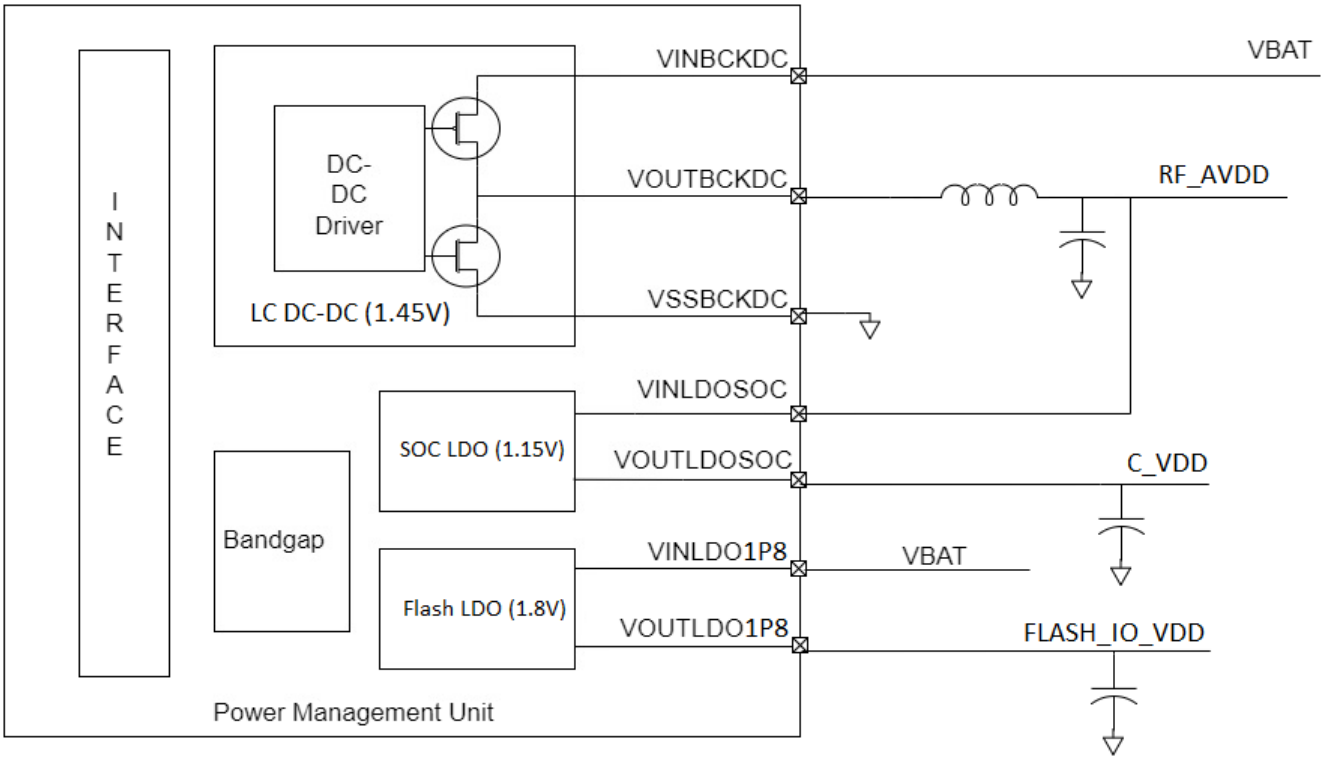


Figure 2.1. Power Management Unit

2.3.1 PMU Modes

Active Mode

PMU can be configured to Active mode through APIs. In the active mode, PMU supports the SOC's maximum power requirement. LC DC-DC (1.45 V) converter works in PWM mode with fixed frequency to achieve high efficiency at high load condition. The LDOs can support their maximum load current.

Sleep Mode

PMU can be configured to Sleep mode through APIs. In the Sleep mode, PMU supports no more than 50 mA current for LC DC-DC (1.45 V) and SOC LDO (1.15 V). LC DC-DC (1.45 V) converter works in PFM mode with variable frequency to achieve high efficiency at low load condition. In this mode, Flash LDO (1.8 V) can support max current.

Ultra Sleep Mode

PMU can be configured to Ultra Sleep mode through APIs. In the Ultra Sleep mode, both the LDOs are turned off and LC DC-DC (1.45 V) is configured in PFM mode. In this mode, the PMU consumes less than 1 µA current and retains the buck output voltage to 1.2 V.

LDO Switch Mode

Both the LDOs can be configured in LDO switch mode through APIs. In LDO switch mode, LDO is bypassed and power MOSFET is used as a switch to pass input voltage directly to the output voltage. It can be configured in PMU active or PMU sleep mode.

2.3.2 Bypass Options

The PMU's internal power converters can be bypassed and supplied by an external source (ULP Regulators cannot be bypassed). This can be beneficial if different devices on the design require/use these voltages. See the following figures:

Note: Register settings mentioned in the bypass options can be set using `PMU_SPI_MEM_MAP(<ipmu_register>)|=<bitmask>;` or cleared by `PMU_SPI_MEM_MAP(<ipmu_register>)&=<bitmask>;`

LC DC-DC (1.45 V) Bypass

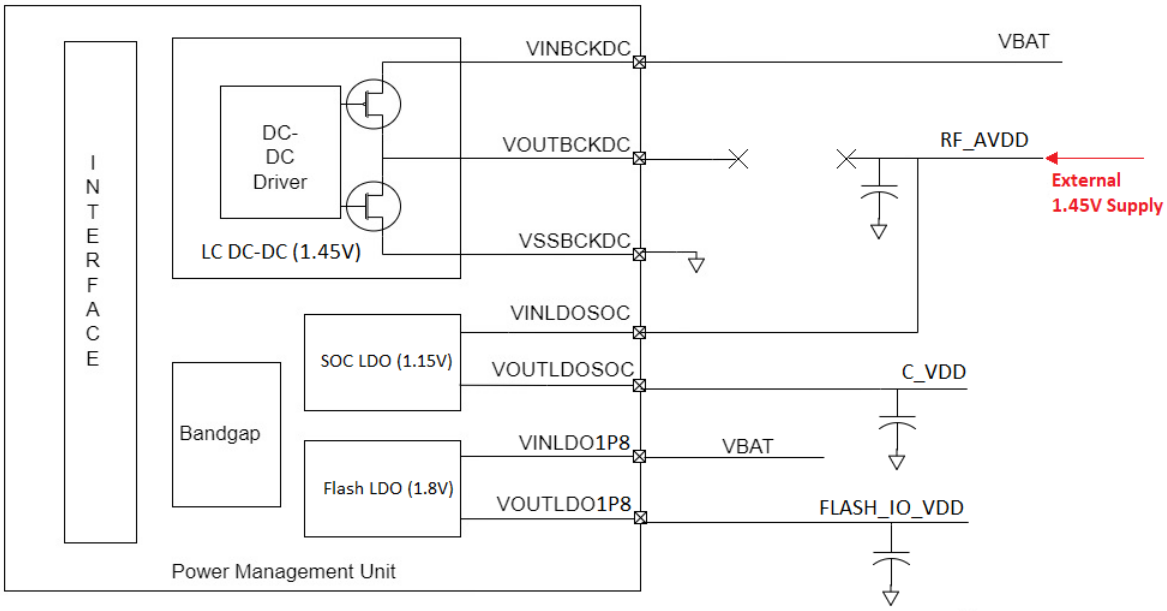


Figure 2.2. LC DC-DC (1.45 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Apply External 1.45 V to VINLDOSOC after a delay of 250 µs.

Registers to set at initialization:

- IPMU Register: 1D0, <20:17> bits should be set to 0b0101.

SOC LDO (1.15 V) Bypass

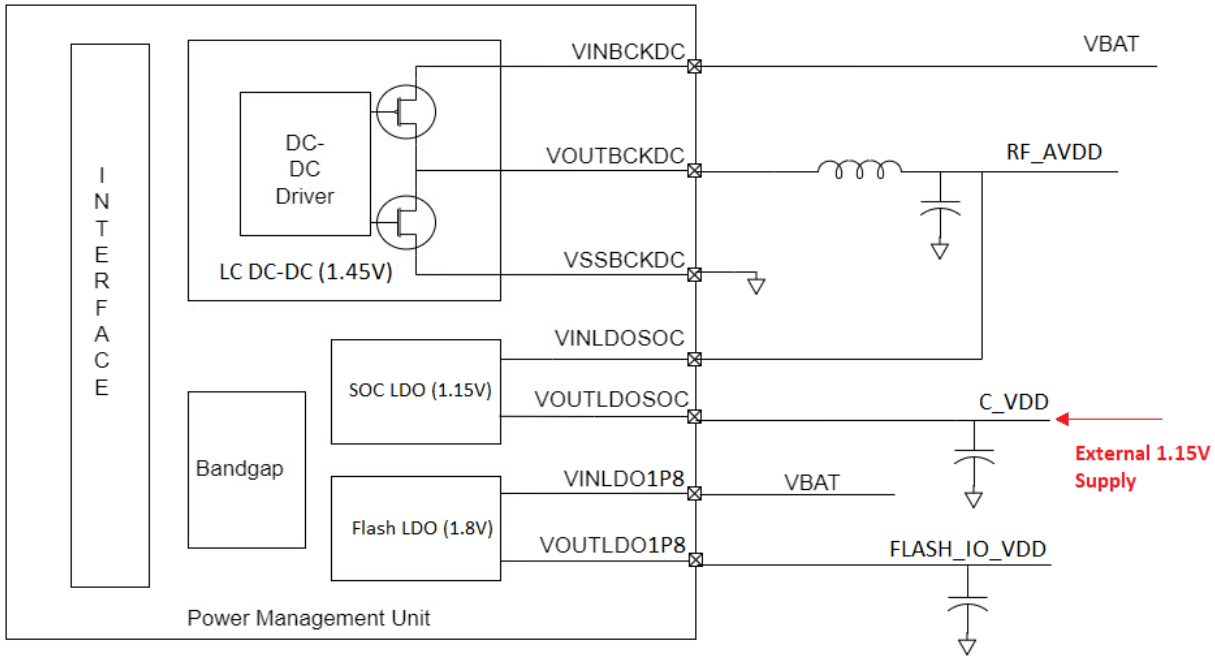


Figure 2.3. SOC LDO (1.15 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Apply External 1.15 V to VOUTLDOSOC after a delay of 600 µs.

Registers to set at initialization:

- IPMU Register: 1D6, 5th bit should be set to 0.
- IPMU Register: 1D6, <3:0> bits should be set to 0b0110.

Flash LDO (1.8 V) Bypass

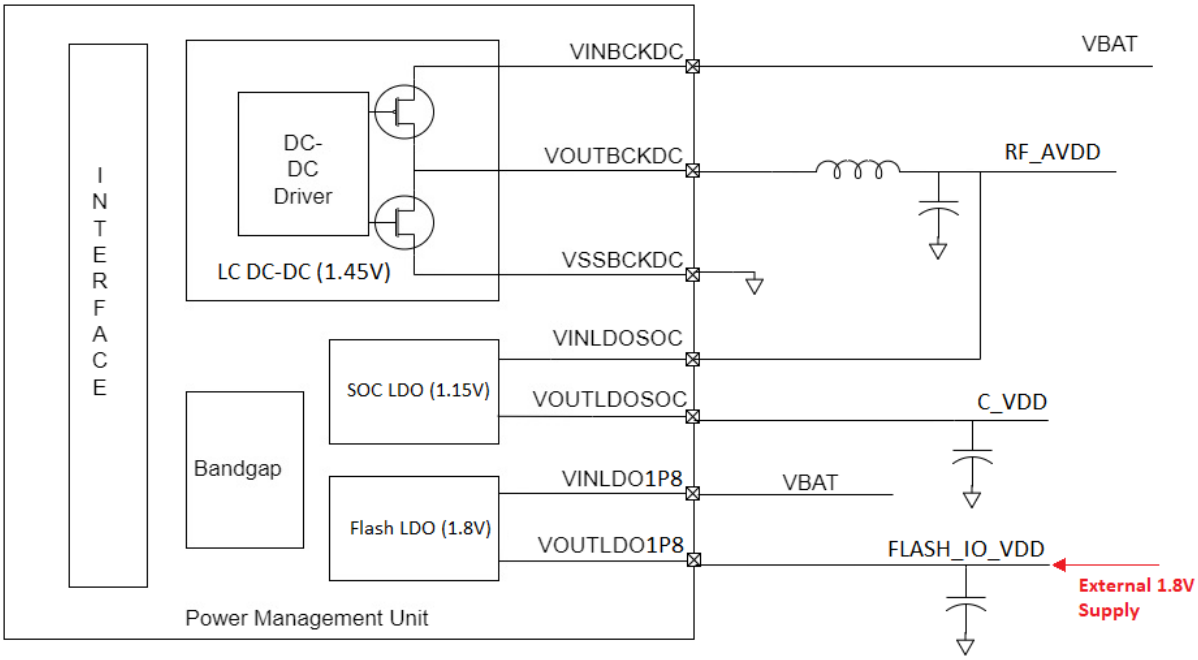


Figure 2.4. Flash LDO (1.8 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Connect VOUTLDO1P8 to 1.8 V external supply after a delay of 250 µs in case Flash supply is 1.8 V.

Registers to set at initialization:

- IPMU Register: 1D6, 11th bit should be set to 0.
- IPMU Register: 1D6, <9:6> bits should be set to 0.

LC DC-DC (1.45 V) +SOC LDO (1.15 V) Bypass

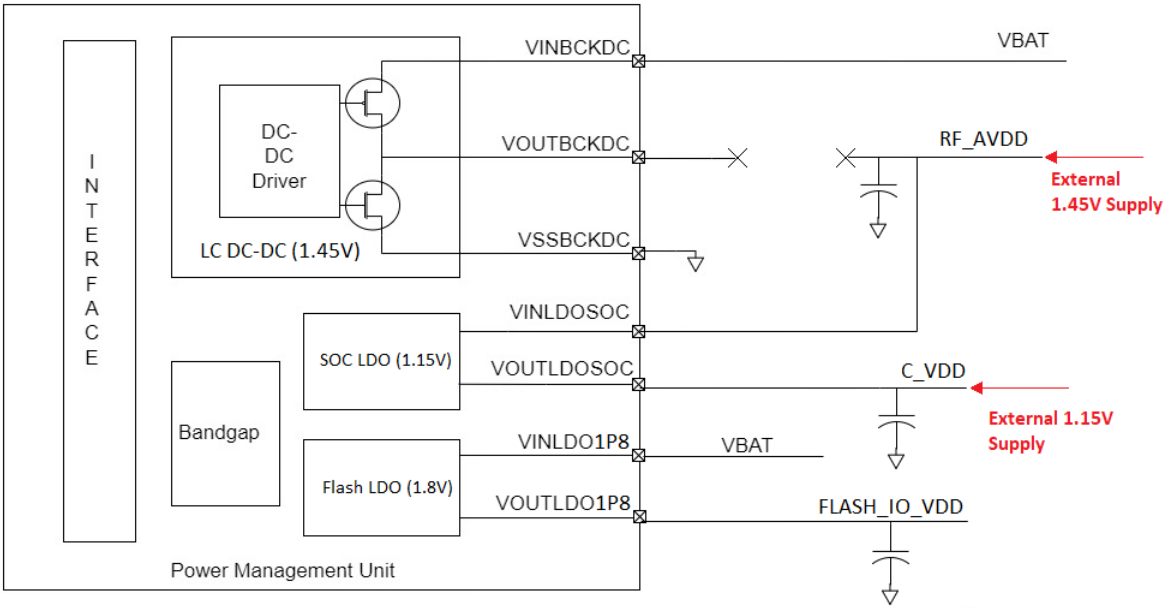


Figure 2.5. LC DC-DC (1.45 V) + SOC LDO (1.15 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Apply external supply of 1.4 V to VINLDOSOC after a delay of 250 µs.
3. Apply external supply of 1.15 V to VOUTLDOSOC after a delay of 600 µs.

Registers to set at initialization:

- IPMU Register: 1D0, <20:17> bits should be set to 0b0101
- IPMU Register: 1D6, 5th bit should be set to 0.
- IPMU Register: 1D6, <3:0> bits should be set to 0b0110.

LC DC-DC (1.45 V) + Flash LDO (1.8 V) Bypass

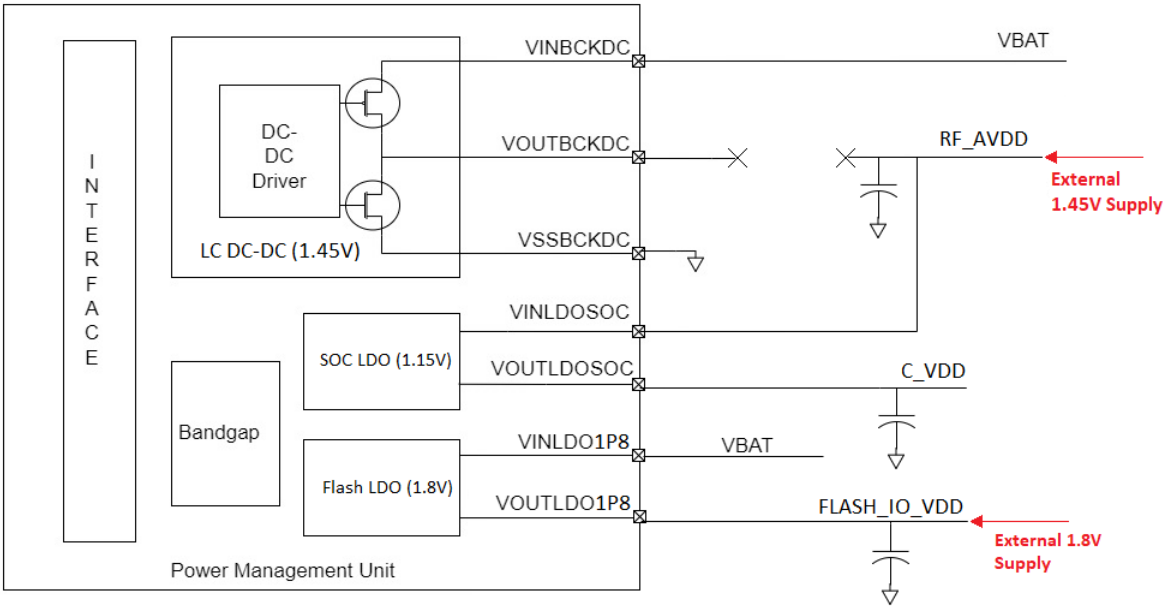


Figure 2.6. LC DC-DC (1.45 V) + Flash LDO (1.8 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Apply External 1.45 V to VINLDOSOC after a delay of 250 µs.
3. Connect VOUTLDO1P8 to 1.8V external supply after a delay of 250 µs in case Flash supply is 1.8 V.

Registers to set at initialization:

- IPMU Register: 1D6, 11th bit should be set to 0.
- IPMU Register: 1D6, <9:6> bits should be set to 0.
- IPMU Register: 1D0, <20:17> bits should be set to 0b0101.

SOC LDO (1.15 V) +Flash LDO (1.8 V) Bypass

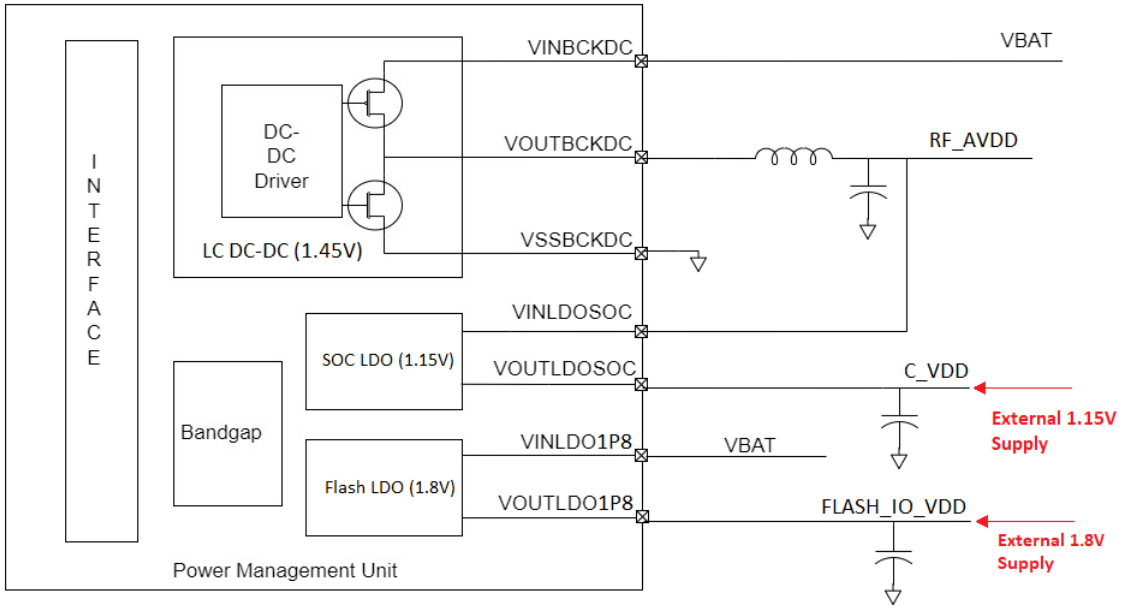


Figure 2.7. SOC LDO (1.15 V) + Flash LDO (1.8 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Apply External 1.15 V to VOUTLDOSOC after a delay of 600 µs.
3. Connect VOUTLDO1P8 to 1.8 V external supply after a of 250 µs in case Flash supply is 1.8 V.

Registers to set at initialization:

- IPMU Register: 1D6, 11th bit should be set to 0.
- IPMU Register: 1D6, <9:6> bits should be set to 0.
- IPMU Register: 1D6, 5th bit should be set to 0.
- IPMU Register: 1D6, <3:0> bits should be set to 0b0110.

LC DC-DC (1.45 V) + SOC LDO (1.15 V) +Flash LDO (1.8 V) Bypass

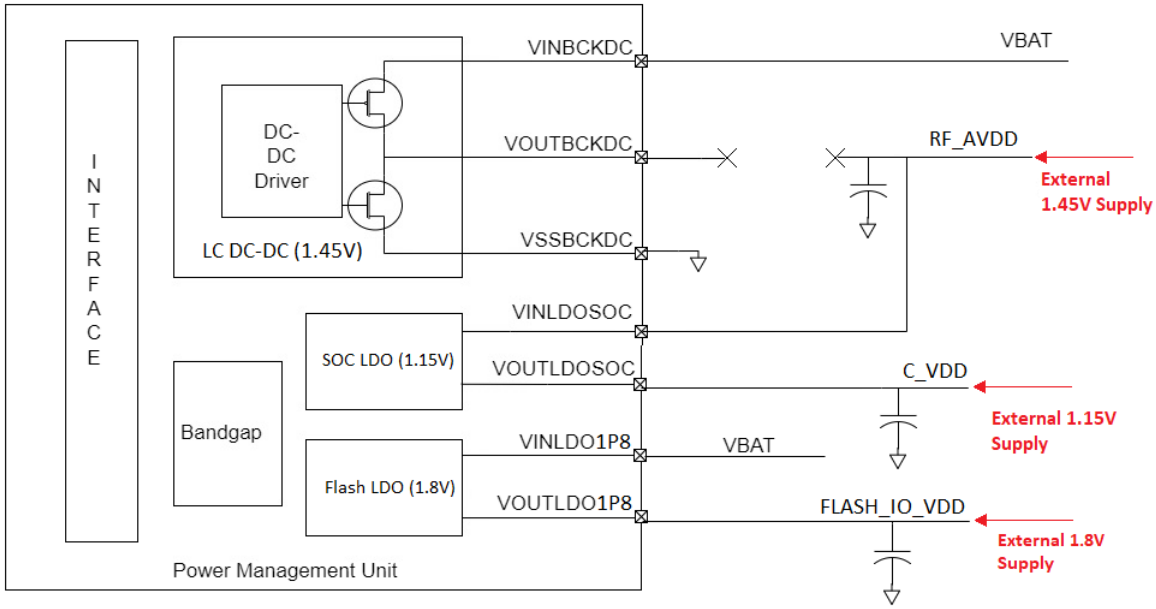


Figure 2.8. LC DC-DC (1.45 V) + SOC LDO (1.15 V) + Flash LDO (1.8 V) Bypass

Power-up sequence:

1. Apply VBAT to VINBCKDC and VINLDO1P8.
2. Apply External 1.45 V to VINLDOSOC after a delay of 250 µs.
3. Apply External 1.15 V to VOUTLDOSOC after a delay of 600 µs.
4. Connect VOUTLDO1P8 to 1.8 V external supply after a delay of 250 µs in case Flash supply is 1.8 V.

Registers to set at initialization:

- IPMU Register: 1D6, 11th bit should be set to 0.
- IPMU Register: 1D6, <9:6> bits should be set to 0.
- IPMU Register: 1D6, 5th bit should be set to 0.
- IPMU Register: 1D6, <3:0> bits should be set to 0b0110.
- IPMU Register: 1D0, <20:17> bits should be set to 0b0101.

2.3.3 Requirements for External Supplies

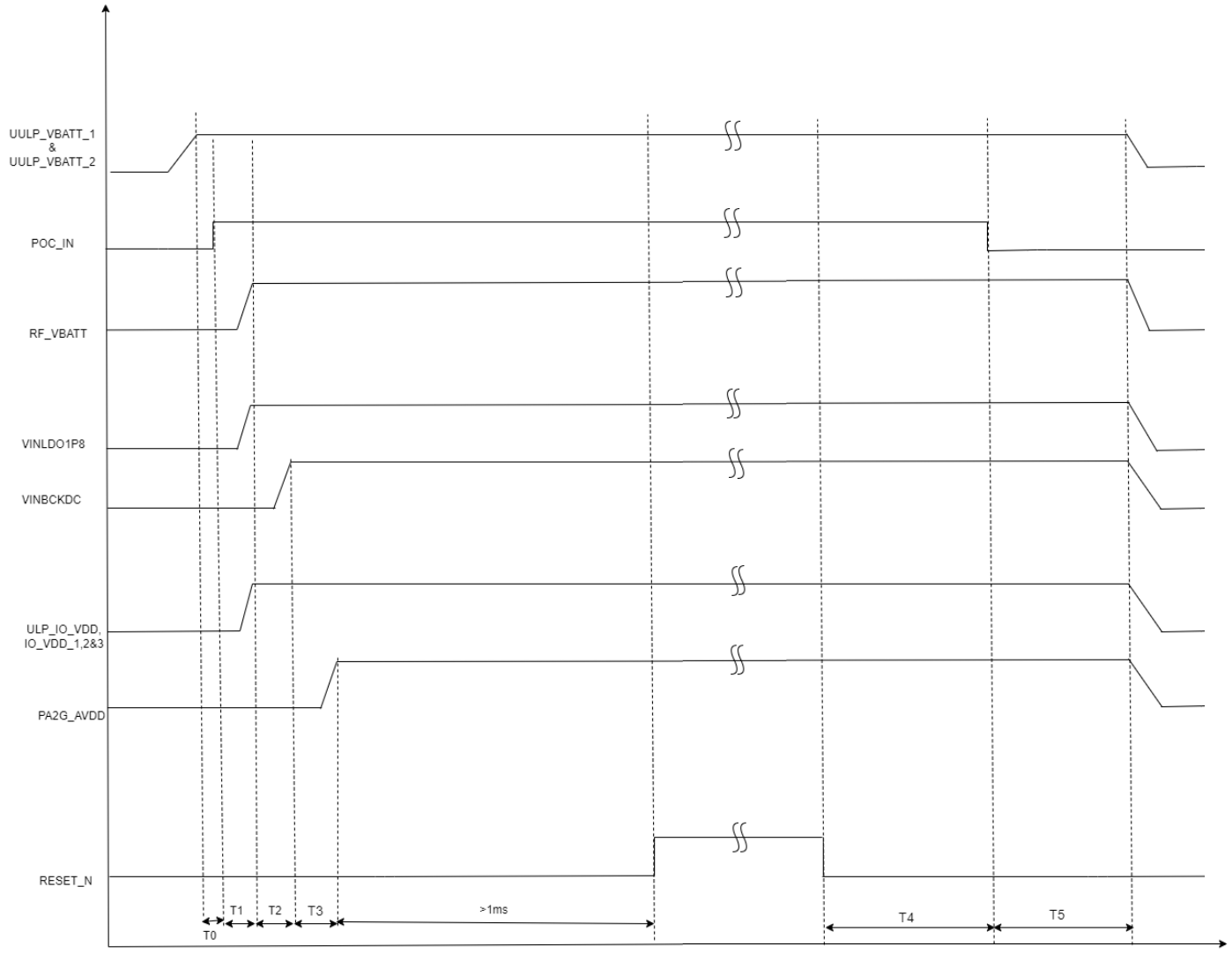
If either the LC DC-DC (1.45 V) or the SOC LDO (1.15 V) is bypassed, the external source that replaces them has to fulfill the requirements stated in the table below. It is important that these are met, as the subsystems supplied by these sources are quite sensitive to unwanted frequency components, higher voltage ripple, etc. The requirements are given for the input pins C_VDD (sourced from SOC LDO) and RF_AVDD (sourced from LC DC-DC).

Table 2.2. Requirements for External Supplies

	C_VDD	RF_AVDD
Voltage Typ.	1.15 V	1.45 V
Voltage Min.	1.05 V	1.35 V
Voltage Max.	1.21 V	1.98 V
Max. Switching Frequency Component	-80 dBV	-70 dBV
Max. Preferred Switching Frequency	1 MHz	1 MHz
Max. Load	300 mA	100 mA
Max. Voltage Ripple	10 mVp-p	20 mVp-p
Worst Load Change	10 mA - 200 mA/ 100 ns	10-50 mA/100 ns

2.4 Power Sequencing

When power supplies are connected individually or internal power converters are bypassed, special care is needed when powering on/off the device. Strict power sequencing must be followed, as shown in the figure below.



1. T1 ,T2 & T3 minimum can be zero.
2. T4 & T5 are >0 us
3. T0 > 600us
4. All supplies (shown in the abode picture) other than UULP_VBATT_1&2 can come earlier or later than POC_IN becoming high
5. There is no particular order between RF_VBATT, VINLDO1P8, ULP_IO_VDD, IO_VDD_1,2&3
6. Rise time of supplies must be > 10us and < 100ms
7. *Once all supplies are stable, RESET_N must be high after >1ms.*

3. Decoupling and Supply Routing Guidelines

3.1 Decoupling Guidelines

The currents drawn by the SiWx917 are low on average but can contain high frequency spikes. These are caused by the digital IO lines and the radio transmission bursts, causing significant noise. This noise needs to be filtered out, otherwise it can compromise receiver performance and cause compatibility issues. This can be solved by decoupling capacitors on the supply and ground traces.

These decoupling capacitors aim to shorten the path for high frequency transients, thus lowering the noise levels. So, they need to be as close to the power supply pins, ground pins, and planes as possible. If multiple decoupling capacitors are needed, the lowest capacitance needs to be the closest to decoupled pin.

Note: Special care should be taken to choose capacitors that have a temperature/voltage range reflecting the operating range of the end device. Certain capacitors, especially those in smaller packages or containing less expensive dielectrics, may undergo a significant decrease in capacitance value with changes in temperature or as the DC bias voltage rises. Any alteration that pushes the capacitor beyond its limits could lead to instability in the supply output.

For capacitor values, see the reference schematics section of the SiWG917 Data Sheet.

3.2 Power Supply Routing Guidelines

To avoid propagation of harmonic frequency components and resonance, follow the guidelines in the latest data sheet and the ones mentioned below:

- Do not share the same routing between PA2G_AVDD and RF_VBATT.
- Use star-routing for PA2G_AVDD and RF_VBATT.
- VOUTBCKDC must be star-routed to RF_AVDD pins.

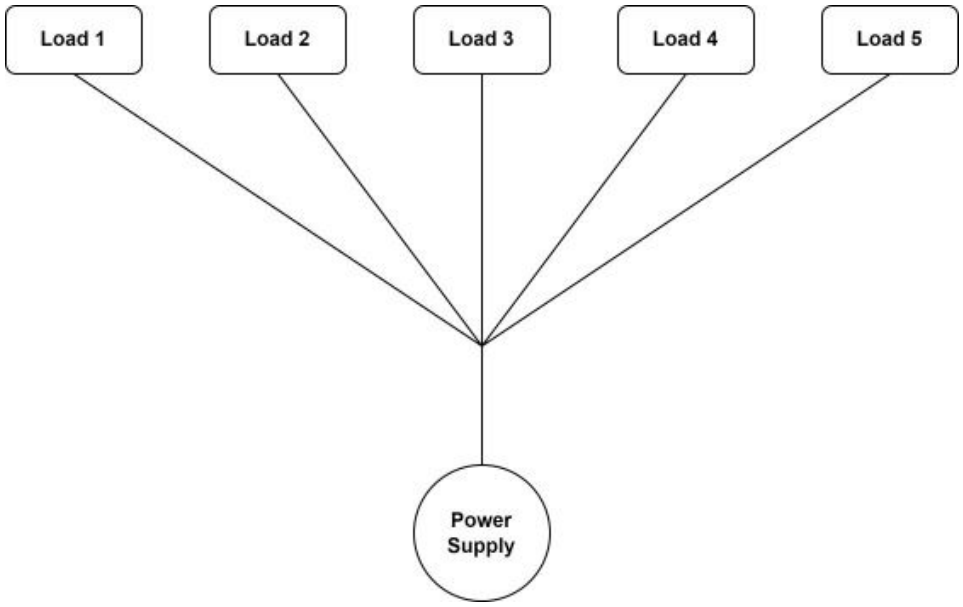


Figure 3.1. Star-routing Topology

For more detailed guidelines on layout and routing, refer to AN1423: SiWx917 RF Matching and Layout Design Guide.

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