Wireless Gecko *Bluetooth*® Module BGM220S Errata

This document contains information on the BGM220S errata. The latest available revision of this device is revision 2.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

Errata effective date: June, 2020.

1. Errata Summary

The table below lists all known errata for the BGM220S and all unresolved errata in revision 2 of the BGM220S.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			1	2
EMU_E303	Watchdog Reset Hangs System Entering EM2 or EM3	Yes	X	X
USART_E301	Possible Data Transmission on Wrong Edge in Synchronous Mode	Yes	X	X
USART_E302	Additional SCLK Pulses Can Be Generated in USART Synchronous Mode	Yes	X	X

2. Current Errata Descriptions

2.1 EMU_E303 – Watchdog Reset Hangs System Entering EM2 or EM3

Description of Errata
The chip can hang and require a hard reset (pin or power-on) to recover if 1. The system is operating with VSCALE1 core voltage scaling (software has previously written a 1 to the EMU_CMD_EM01VSCALE1 bit), 2. The system is in the process or entering EM2 or EM3 (software has just executed the WFE or WFI instruction with the SLEEPDEEP bit in the System Control Register set) and 3. A Watchdog timeout reset is triggered
Affected Conditions / Impacts
Systems operating with core voltage scaling can hang if a Watchdog reset occurs immediately upon EM2 or EM3 entry.
Workaround
Systems that keep the Watchdog enabled in low energy modes should, as a matter of good programming practice, service the Watchdog before entering EM2 or EM3. Calling the emlib `WDOGn_Feed()` function followed by the `WDOGn_SyncWait()` function (to ensure that the servicing write to the WDOG_CMD register completes execution) immediately before entering EM2 or EM3 will prevent a Watchdog reset that could possibly hang the system under the specified circumstances.
Resolution
There is currently no resolution for this issue.

2.2 USART_E301 — Possible Data Transmission on Wrong Edge in Synchronous Mode

Description of Errata
The first bit of the new data word is incorrectly transmitted on the leading clock edge of the subsequent data bit and not the trailing clock edge of the current data bit if the USART is configured to operate in synchronous mode with 1. USART_CLKDIV_DIV = 0 (clock = $f_{HFPERCLK} \div 2$), 2. USART_CTRL_CLKPHA = 0, 3. USART_TIMING_CSHOLD = 1 and 4. Data is loaded into the transmit FIFO (say, by the LDMA) at the exact same time as the USART state machine begins to insert the requested one bit time extension of the chip select hold time (USART_TIMING_CSHOLD = 1).
Affected Conditions / Impacts
Reception of each data bit by the slave is tied to a specific clock edge. Therefore, the late transmission by the master of the first bit of a word may cause the slave to receive the incorrect data, especially if the data setup time for the slave approaches or exceeds one half the shift clock period.
Workaround
Because there is no way to specifically time a write to the transmit FIFO such that it does not occur when the USART state machine changes state, use one of the following workarounds to avoid the risk for data corruption described above: • Set USART_CLK_DIV > 0. • Use USART_TIMING_CSHOLD = 0 or USART_TIMING_CSHOLD > 1. • Use USART_CTRL_CLKPHA = 1. This is option is particularly useful with SPI flash memories as many support operation in both the CLKPOL = CLKPHA = 0 and CLKPOL = CLKPHA = 1 modes.
Resolution
There is currently no resolution for this issue.

2.3 USART_E302 — Additional SCLK Pulses Can Be Generated in USART Synchronous Mode

Description of Errata
When inter-character spacing is enabled (USART_TIMING_ICS > 0) and USART_CTRL_CLKPHA = 1 in synchronous master mode, an extra clock pulse is generated after each frame transmitted except the last (that frame which when sent results in both the transmit FIFO and transmit shift register being empty).
Affected Conditions / Impacts
The extra clock pulse generated at the end of the first frame would cause a slave device to clock in the first bit of the next frame it expects to receive even though the USART is not yet driving that data. The slave would lose synchronization with the master and erroneously receive all frames after the first.
Workaround
Do not enable inter-character spacing when CLKPHA = 1. If a delay between frames is necessary, insert one manually with a software delay loop. Data cannot be transmiited using DMA in this case.
Resolution
There is currently no resolution for this issue.

3. Revision History

Revision 0.1

June, 2020

- Initial release.

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