



# Wireless Gecko *Bluetooth*® Module BGM220P Errata

---



This document contains information on the BGM220P errata. The latest available revision of this device is revision 2.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

Errata effective date: June, 2020.

## 1. Errata Summary

The table below lists all known errata for the BGM220P and all unresolved errata in revision 2 of the BGM220P.

**Table 1.1. Errata Overview**

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			1	2
EMU_E303	<a href="#">Watchdog Reset Hangs System Entering EM2 or EM3</a>	Yes	X	X
USART_E301	<a href="#">Possible Data Transmission on Wrong Edge in Synchronous Mode</a>	Yes	X	X
USART_E302	<a href="#">Additional SCLK Pulses Can Be Generated in USART Synchronous Mode</a>	Yes	X	X

## 2. Current Errata Descriptions

### 2.1 EMU\_E303 – Watchdog Reset Hangs System Entering EM2 or EM3

<b>Description of Errata</b>
<p>The chip can hang and require a hard reset (pin or power-on) to recover if</p> <ol style="list-style-type: none"> <li>1. The system is operating with VSCALE1 core voltage scaling (software has previously written a 1 to the EMU_CMD_EM01VSCALE1 bit),</li> <li>2. The system is in the process or entering EM2 or EM3 (software has just executed the WFE or WFI instruction with the SLEEP-DEEP bit in the System Control Register set) and</li> <li>3. A Watchdog timeout reset is triggered</li> </ol>
<b>Affected Conditions / Impacts</b>
Systems operating with core voltage scaling can hang if a Watchdog reset occurs immediately upon EM2 or EM3 entry.
<b>Workaround</b>
Systems that keep the Watchdog enabled in low energy modes should, as a matter of good programming practice, service the Watchdog before entering EM2 or EM3. Calling the <code>emlib WDOGn_Feed()</code> function followed by the <code>WDOGn_SyncWait()</code> function (to ensure that the servicing write to the WDOG_CMD register completes execution) immediately before entering EM2 or EM3 will prevent a Watchdog reset that could possibly hang the system under the specified circumstances.
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.2 USART\_E301 — Possible Data Transmission on Wrong Edge in Synchronous Mode

<b>Description of Errata</b>
<p>The first bit of the new data word is incorrectly transmitted on the leading clock edge of the subsequent data bit and not the trailing clock edge of the current data bit if the USART is configured to operate in synchronous mode with</p> <ol style="list-style-type: none"> <li>1. USART_CLKDIV_DIV = 0 (clock = <math>f_{HFPERCLK} \div 2</math>),</li> <li>2. USART_CTRL_CLKPHA = 0,</li> <li>3. USART_TIMING_CSHOLD = 1 and</li> <li>4. Data is loaded into the transmit FIFO (say, by the LDMA) at the exact same time as the USART state machine begins to insert the requested one bit time extension of the chip select hold time (USART_TIMING_CSHOLD = 1).</li> </ol>
<b>Affected Conditions / Impacts</b>
Reception of each data bit by the slave is tied to a specific clock edge. Therefore, the late transmission by the master of the first bit of a word may cause the slave to receive the incorrect data, especially if the data setup time for the slave approaches or exceeds one half the shift clock period.
<b>Workaround</b>
<p>Because there is no way to specifically time a write to the transmit FIFO such that it does not occur when the USART state machine changes state, use one of the following workarounds to avoid the risk for data corruption described above:</p> <ul style="list-style-type: none"> <li>• Set USART_CLK_DIV &gt; 0.</li> <li>• Use USART_TIMING_CSHOLD = 0 or USART_TIMING_CSHOLD &gt; 1.</li> <li>• Use USART_CTRL_CLKPHA = 1. This option is particularly useful with SPI flash memories as many support operation in both the CLKPOL = CLKPHA = 0 and CLKPOL = CLKPHA = 1 modes.</li> </ul>
<b>Resolution</b>
There is currently no resolution for this issue.

## 2.3 USART\_E302 — Additional SCLK Pulses Can Be Generated in USART Synchronous Mode

<b>Description of Errata</b>
When inter-character spacing is enabled (USART_TIMING_ICS > 0) and USART_CTRL_CLKPHA = 1 in synchronous master mode, an extra clock pulse is generated after each frame transmitted except the last (that frame which when sent results in both the transmit FIFO and transmit shift register being empty).
<b>Affected Conditions / Impacts</b>
The extra clock pulse generated at the end of the first frame would cause a slave device to clock in the first bit of the next frame it expects to receive even though the USART is not yet driving that data. The slave would lose synchronization with the master and erroneously receive all frames after the first.
<b>Workaround</b>
Do not enable inter-character spacing when CLKPHA = 1. If a delay between frames is necessary, insert one manually with a software delay loop. Data cannot be transmitted using DMA in this case.
<b>Resolution</b>
There is currently no resolution for this issue.

### 3. Revision History

#### Revision 0.1

June, 2020

- Initial release.

# Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!



IoT Portfolio

[www.silabs.com/iot](http://www.silabs.com/iot)



SW/HW

[www.silabs.com/simplicity](http://www.silabs.com/simplicity)



Quality

[www.silabs.com/quality](http://www.silabs.com/quality)



Support & Community

[www.silabs.com/community](http://www.silabs.com/community)

## Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required, or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

## Trademark Information

Silicon Laboratories Inc., Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, ClockBuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR®, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>