EFM32 Gecko
EFM32PG22 Errata

This document contains information on the EFM32PG22 errata. The latest available revision of this device is revision C.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: August, 2020.

1. Errata Summary

The table below lists all known errata for the EFM32PG22 and all unresolved errata in revision C of the EFM32PG22.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:
			C
EMU_E303	Watchdog Reset Hangs System Entering EM2 or EM3	Yes	X
I2C_E303	I2C Fails to Indicate New Incoming Data	Yes	X
TIMER_E301	Continuous Overflow and Underflow Interrupts in Quadrature Counting Mode	Yes	X
USART_E301	Possible Data Transmission on Wrong Edge in Synchronous Mode	Yes	X
USART_E302	Additional SCLK Pulses Can Be Generated in USART Synchronous Mode	Yes	X

2. Current Errata Descriptions

2.1 EMU_E303 – Watchdog Reset Hangs System Entering EM2 or EM3

Description of Errata
The chip can hang and require a hard reset (pin or power-on) to recover if: 1. The system is operating with VSCALE1 core voltage scaling (software has previously written a 1 to the EMU_CMD_EM01VSCALE1 bit), 2. The system is in the process or entering EM2 or EM3 (software has just executed the WFE or WFI instruction with the SLEEPDEEP bit in the System Control Register set), and 3. A Watchdog timeout reset is triggered.
Affected Conditions / Impacts
Systems operating with core voltage scaling can hang if a Watchdog reset occurs immediately upon EM2 or EM3 entry.
Workaround
Systems that keep the Watchdog enabled in low energy modes should, as a matter of good programming practice, service the Watchdog before entering EM2 or EM3. Calling the emlib `WDOGn_Feed()` function followed by the `WDOGn_SyncWait()` function (to ensure that the servicing write to the WDOG_CMD register completes execution) immediately before entering EM2 or EM3 will prevent a Watchdog reset that could possibly hang the system under the specified circumstances.
Resolution
There is currently no resolution for this issue.

2.2 I2C_E303 – I²C Fails to Indicate New Incoming Data

Description of Errata
A race condition exists in which the I²C fails to indicate reception of new data when both user software attempts to read data from and the I²C hardware attempts to write data to the I2C_RXFIFO in the same cycle.
Affected Conditions / Impacts
When this race condition occurs, the RXFIFO enters an invalid state in which both I2C_STATUS_RXDATAV = 0 and I2C_STATUS_RXFULL = 1. This causes the I²C to discard new incoming data bytes because RXFULL = 1 and would otherwise prevent user software from reading last byte written by the I²C hardware to RXFIFO because RXDATAV = 0.
Workaround
User software can recognize and clear this invalid RXDATAV = 0 and RXFULL = 1 condition by performing a dummy read of the RXFIFO (I2C_RXDATA). This restores the expected RXDATAV = 1 and RXFULL = 0 condition. The data from this read can be discarded, and user software can now read the last byte written by the I²C hardware to the RXFIFO (the byte which caused the invalid RXDATAV = 0 and RXFULL = 1 condition). No data will be lost as long as user software completes this recovery procedure (performing the dummy read and then reading the remaining valid byte in the RXFIFO) before the I²C hardware receives the next incoming data byte.
Resolution
There is currently no resolution for this issue.

2.3 TIMER_E301 — Continuous Overflow and Underflow Interrupts in Quadrature Counting Mode

Description of Errata
When the TIMER is configured to operate in quadrature decoder mode with the overflow interrupt enabled and the counter value (TIMER_CNT) reaches the top value (TIMER_TOP), the overflow interrupt is requested contiunously even if the interrupt flag (TIMER_IF_OF) is cleared. Similarly, if the underflow interrupt is enabled and the counter value reaches zero, the underflow interrupt is requested contiunously even if the interrupt flag (TIMER_IF_UF) is cleared. Only after the counter value has incremented or decremented so that the overflow or underflow condition no longer applies can the interrupt be cleared.
Affected Conditions / Impacts
Because the counter is clocked by its CC0 and CC1 inputs in quadrature decoder mode and not the prescaled HFPERCLK, overflow and underflow events remain latched as long TIMER_CNT remains at the value that triggered the overflow or underflow condition. Until the counter is no longer in the overflow or underflow condition, it is not possible to clear the associated interrupt flag.
Workaround

Short of disabling the relevant interrupts, the simplest workaround is to manually increment or decrement TIMER_CNT so that the overflow or underflow condition no longer exists. Insert the following or similar code in the interrupt handler for the timer in question (TIMER0 in this case) to do this:
`uint32 intflags = TIMER_IntGet(TIMER0);`
 	
`if (intFlags & TIMER_IEN_OF)`
`  TIMER0->CNT += 1;`
 	
`if (intFlags & TIMER_IEN_UF)`
`  TIMER0->CNT -= 1;`
 	
It may be necessary for firmware to account for this adjustment in calculations that include the counter value.

Resolution
There is currently no resolution for this issue.

2.4 USART_E301 — Possible Data Transmission on Wrong Edge in Synchronous Mode

Description of Errata
The first bit of the new data word is incorrectly transmitted on the leading clock edge of the subsequent data bit and not the trailing clock edge of the current data bit if the USART is configured to operate in synchronous mode with 1. USART_CLKDIV_DIV = 0 (clock = $f_{HFPERCLK}$ ÷ 2), 2. USART_CTRL_CLKPHA = 0, 3. USART_TIMING_CSHOLD = 1 and 4. Data is loaded into the transmit FIFO (say, by the LDMA) at the exact same time as the USART state machine begins to insert the requested one bit time extension of the chip select hold time (USART_TIMING_CSHOLD = 1).
Affected Conditions / Impacts
Reception of each data bit by the slave is tied to a specific clock edge. Therefore, the late transmission by the master of the first bit of a word may cause the slave to receive the incorrect data, especially if the data setup time for the slave approaches or exceeds one half the shift clock period.
Workaround
Because there is no way to specifically time a write to the transmit FIFO such that it does not occur when the USART state machine changes state, use one of the following workarounds to avoid the risk for data corruption described above: • Set USART_CLK_DIV > 0. • Use USART_TIMING_CSHOLD = 0 or USART_TIMING_CSHOLD > 1. • Use USART_CTRL_CLKPHA = 1. This option is particularly useful with SPI flash memories as many support operation in both the CLKPOL = CLKPHA = 0 and CLKPOL = CLKPHA = 1 modes.
Resolution
There is currently no resolution for this issue.

2.5 USART_E302 — Additional SCLK Pulses Can Be Generated in USART Synchronous Mode

Description of Errata
When inter-character spacing is enabled (USART_TIMING_ICS > 0) and USART_CTRL_CLKPHA = 1 in synchronous master mode, an extra clock pulse is generated after each frame transmitted except the last (that frame which when sent results in both the transmit FIFO and transmit shift register being empty).
Affected Conditions / Impacts
The extra clock pulse generated at the end of the first frame would cause a slave device to clock in the first bit of the next frame it expects to receive even though the USART is not yet driving that data. The slave would lose synchronization with the master and erroneously receive all frames after the first.
Workaround
Do not enable inter-character spacing when CLKPHA = 1. If a delay between frames is necessary, insert one manually with a software delay loop. Data cannot be transmiited using DMA in this case.
Resolution
There is currently no resolution for this issue.

3. Revision History

Revision 0.1

August, 2020

- Initial release.

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