



# Gecko

## EFM32PG23 Errata

---



This document contains information on the EFM32PG23 errata. The latest available revision of this device is revision C.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from the package marking or electronically.

Errata effective date: April, 2022.

## 1. Errata Summary

The table below lists all known errata for the EFM32PG23 and all unresolved errata in revision C of the EFM32PG23.

**Table 1.1. Errata Overview**

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			B	C
CUR_E302	Extra EM1 Current if FPU is Disabled	Yes	X	X
CUR_E303	Active Charge Pump Clock Causes High Current	Yes	X	—
DCDC_E302	DCDC Interrupts Block EM2/3 Entry or Cause Unexpected Wake-up	Yes	X	X
EMU_E305	DC-DC Refresh Time Delay	Yes	X	X
IADC_E305	FIFO Cannot Detect Eighth Entry	Yes	X	X
IADC_E306	Changing Gain During a Scan Sequence Causes an Erroneous IADC Result	Yes	X	X
KEYSCAN_E301	Unused Rows Are Not Properly Gated Off	Yes	X	X
USART_E304	PRS Transmit Unavailable in Synchronous Secondary Mode	No	X	X

## 2. Current Errata Descriptions

### 2.1 CUR\_E302 – Extra EM1 Current if FPU is Disabled

<b>Description of Errata</b>
When the Floating Point Unit (FPU) is disabled, the on-demand Fast Startup RC Oscillator (FSRCO) remains on after an energy mode transition from EM0 to EM1 is complete. This leads to higher current consumption in EM1.
<b>Affected Conditions / Impacts</b>
The enabled FSRCO increases EM1 current consumption by ~500 µA.
<b>Workaround</b>
Always enable the FPU at the beginning of code execution via the Coprocessor Access Control Register (CPACR) in the System Control Block (SCB) as shown below:
<pre>SCB-&gt;CPACR  = ((3 &lt;&lt; 20)   (3 &lt;&lt; 22));</pre>
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.2 DCDC\_E302 – DCDC Interrupts Block EM2/3 Entry or Cause Unexpected Wake-up

<b>Description of Errata</b>
Regardless of DCDC_IEN setting, if the DCDC interrupt is enabled in the NVIC, any of the four DCDC interrupt sources (DCDC_IF_WARM, DCDC_IF_RUNNING, DCDC_IF_TMAX, and DCDC_IF_BYPSW) can wake the device from EM2/3 or prevent it from entering EM2/3.
<b>Affected Conditions / Impacts</b>
The errata is limited to the DCDC_IF_WARM, DCDC_IF_RUNNING, DCDC_IF_TMAX and DCDC_IF_BYPSW requests, which also function as wake-up sources from EM2/3.
When the NVIC DCDC interrupt source is enabled:
<ul style="list-style-type: none"> <li>• If IEN for one of these interrupt requests is set to 1 and that condition occurs, then an interrupt <i>*will*</i> occur and the CPU will branch to the DCDC IRQ handler.</li> <li>• If IEN for one of these interrupt sources is cleared to 0 and that condition occurs, then an interrupt <i>*will not*</i> occur.</li> <li>• If any of these four interrupt conditions occurs, regardless of the setting of their corresponding DCDC_IEN bits, the device <i>*will*</i> wake from EM2/3 and/or be prevented from entering EM2/3. If the corresponding IEN was not set, an interrupt <i>*will not*</i> occur even though the EM2/3 wakeup event has occurred.</li> </ul>
<b>Workaround</b>
To prevent unwanted wake-up from or blocked entry into EM2/3, disable the DCDC interrupt using <code>NVIC_DisableIRQ(DCDC_IRQn)</code> before entering EM2/3 and re-enable the DCDC interrupt using <code>NVIC_EnableIRQ(DCDC_IRQn)</code> after EM2/3 wake-up.
<b>Resolution</b>
There is currently no resolution for this issue.

## 2.3 EMU\_E305 – DC-DC Refresh Time Delay

<b>Description of Errata</b>
The DC-DC fast refresh delay required after exiting EM2/3 and entering continuous conduction mode (CCM) is not honored.
<b>Affected Conditions / Impacts</b>
When the system exits EM2/3 and the DC-DC is set to CCM, the DC-DC voltage comparator needs to be refreshed. This refresh delay is not honored when exiting EM2/3.
<b>Workaround</b>
Firmware must wait for at least 20 $\mu$ s before enabling DCDC CCM upon wake from EM2/3.
<b>Resolution</b>
There is currently no resolution for this issue.

## 2.4 IADC\_E305 – FIFO Cannot Detect Eighth Entry

<b>Description of Errata</b>
The IADC is unable to detect when the eighth FIFO entry has been loaded and will not set the corresponding SINGLEFIFODVL or SCANFIFODVL flag in the IADC_IF register or request LDMA service.
<b>Affected Conditions / Impacts</b>
If the DVL field of IADC_SINGLEFIFOCFG or IADC_SCANFIFOCFG is set to VALID8, a FIFO full condition is not registered when the eighth FIFO entry is loaded. In particular, this means that if the LDMA is configured to empty the FIFO when it is filled with eight entries, the LDMA will never issue a request to perform the transfers necessary to do this.
Similarly, the IADC will not set the IADC_IF_SINGLEFIFODVL or IADC_IF_SCANFIFODVL to request an interrupt in response to the FIFO being filled with eight entries.
<b>Workaround</b>
Do not configure the IADC to request an interrupt or LDMA service when all eight entries are full (IADC_SINGLEFIFOCFG_DVL = VALID8 or IADC_SCANFIFOCFG_DVL = VALID8). All other settings of the DVL field (VALID1 to VALID7) operate as expected.
<b>Resolution</b>
There is currently no resolution for this issue.

## 2.5 IADC\_E306 – Changing Gain During a Scan Sequence Causes an Erroneous IADC Result

<b>Description of Errata</b>
Differences in the ANALOGGAIN setting within multiple IADC_CFGx groups during a scan sequence introduces a transient condition that may result in an inaccurate IADC conversion.
<b>Affected Conditions / Impacts</b>
The result of the IADC scan measurement may not match the expected result for the voltage present on the pin during the conversion.
<b>Workaround</b>
Both 1 and 2 shown below must be implemented. <ol style="list-style-type: none"> <li>1. If there is a difference in the ANALOGGAIN setting between IADC_CFGx groups during a scan sequence, the IADC_SCHEx clock prescaler must also change to an appropriate setting. This forces a warmup state (5 <math>\mu</math>s delay) in between ANALOGGAIN changes. Note that the same IADC_SCHEx clock prescaler value may be an appropriate setting for both ANALOGGAIN settings, but to force the warmup delay, the IADC_SCHEx must have different values.</li> <li>2. The first and last entry of a scan group should use IADC_CFG0, which is the default configuration of the IADC at the start and end of a scan conversion sequence. If CONFIG1 is used at the start and end of the scan group, erroneous IADC results may occur.</li> </ol>
<b>Resolution</b>
There is currently no resolution for this issue.

## 2.6 KEYSCAN\_E301 – Unused Rows Are Not Properly Gated Off

Description of Errata
Unused KEYSCAN row inputs cause the KEY bit in the KEYSCAN_IF register to be set at all times indicating a key was pressed. This prevents the interrupt flag from clearing and stops the scan procedure.
Affected Conditions / Impacts
The KEY bit in the KEYSCAN_IF register is always set when rows are left unused.
Workaround
Configure the GPIO_KEYSCAN_ROWSENSEnROUTE registers for any unused row inputs to the same GPIO port and pin associated with any of the row inputs that are used. For example, if rows 0, 1, and 2 are used and routed to PA05, PA06, and PA07 respectively, and rows 3, 4, and 5 are unused, the configuration could be:
<pre>// Routing GPIO pins PA05, PA06 and PA07 to rows 0, 1 and 2 GPIO-&gt;DBUSKEYPAD_ROWSENSE0ROUTE = 0 &lt;&lt; _GPIO_DBUSKEYPAD_ROWSENSE0ROUTE_PORT_SHIFT   5 &lt;&lt; _GPIO_DBUSKEYPAD_ROWSENSE0ROUTE_PIN_SHIFT; GPIO-&gt;DBUSKEYPAD_ROWSENSE1ROUTE = 0 &lt;&lt; _GPIO_DBUSKEYPAD_ROWSENSE1ROUTE_PORT_SHIFT   6 &lt;&lt; _GPIO_DBUSKEYPAD_ROWSENSE1ROUTE_PIN_SHIFT; GPIO-&gt;DBUSKEYPAD_ROWSENSE2ROUTE = 0 &lt;&lt; _GPIO_DBUSKEYPAD_ROWSENSE2ROUTE_PORT_SHIFT   7 &lt;&lt; _GPIO_DBUSKEYPAD_ROWSENSE2ROUTE_PIN_SHIFT;  // Workaround - Connect unused rows 3, 4, and 5 to row 2 (PA07), a single used row GPIO-&gt;KEYPADROUTE_ROWSENSE3ROUTE = 0 &lt;&lt; _GPIO_KEYSCAN_ROWSENSE3ROUTE_PORT_SHIFT   7 &lt;&lt; _GPIO_KEYSCAN_ROWSENSE3ROUTE_PIN_SHIFT; GPIO-&gt;KEYPADROUTE_ROWSENSE4ROUTE = 0 &lt;&lt; _GPIO_KEYSCAN_ROWSENSE4ROUTE_PORT_SHIFT   7 &lt;&lt; _GPIO_KEYSCAN_ROWSENSE4ROUTE_PIN_SHIFT; GPIO-&gt;KEYPADROUTE_ROWSENSE5ROUTE = 0 &lt;&lt; _GPIO_KEYSCAN_ROWSENSE5ROUTE_PORT_SHIFT   7 &lt;&lt; _GPIO_KEYSCAN_ROWSENSE5ROUTE_PIN_SHIFT;</pre>
Note that KEYSCAN_STATUS.ROW will report the same values for used and unused rows that route to the same GPIO. In the scenario above, KEYSCAN_STATUS.ROW bits 2, 3, 4, and 5 will show the same values. The unused row bits in the KEYSCAN_STATUS field should be masked so that unused row bits are set to 1, indicating a key is not pressed.
Resolution
There is currently no resolution for this issue.

## 2.7 USART\_E304 — PRS Transmit Unavailable in Synchronous Secondary Mode

Description of Errata
When the USART is configured for synchronous secondary operation, the transmit output (MISO) is not driven if the signal is routed to a pin using the PRS producer (e.g., SOURCESEL = 0x20 and SIGSEL = 0x4 for USART0).
Affected Conditions / Impacts
Systems cannot operate the USART in synchronous secondary mode if the PRS is used to route the transmit output to the RX (MISO) pin. Operation is not affected in main mode when the transmit output is routed to the TX (MOSI) pin using the PRS producer nor is operation affected in any mode when the GPIO_USARTn_RXROUTE and GPIO_USARTn_TXROUTE registers are used.
Workaround
There is currently no workaround for this issue.
Resolution
There is currently no resolution for this issue.

### 3. Resolved Errata Descriptions

This section contains previous errata for EFM32PG23 devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

#### 3.1 CUR\_E303 – Active Charge Pump Clock Causes High Current

<b>Description of Errata</b>
When the ACMP0, ACMP1, or IADC0 peripherals are active, the clock to the internal analog mux charge pump may also be activated, resulting in extra supply current.
<b>Affected Conditions / Impacts</b>
<ul style="list-style-type: none"><li>ACMP0 and ACMP1: The charge pump clock is activated whenever either module is enabled via the ACMPn_EN_EN bit or when enabled by the LESENSE state machine.</li><li>IADC0: The charge pump clock is activated when any portion of the IADC analog circuitry is on. When IADC_CTRL_WARMUPMODE = KEEPINSTANDBY or KEEPWARM, the clock is activated as long as the IADC is enabled via the IADC_EN_EN bit. When IADC_CTRL_WARMUPMODE = NORMAL, the clock is activated only during warmup and conversion and will be shut down between conversions.</li><li>The extra current is from a shared block and increases supply current by an approximate total of 25 <math>\mu</math>A when any of the above conditions are true.</li></ul>
<b>Workaround</b>
No workaround exists to entirely eliminate the extra current. The impact of the current can be reduced by duty-cycling the peripheral. The average system supply current increase depends on the total percentage of time the peripheral(s) is/are active. For example, if only ACMP0 is used and enabled for 10% of the time, the average supply current increase is about 2.5 $\mu$ A.
<b>Resolution</b>
This issue is resolved on revision C devices.

## 4. Revision History

### Revision 0.3

April, 2022

- Updated latest device revision to revision C.
- Added [IADC\\_E306](#) and [KEYSCAN\\_E301](#).
- Resolved [CUR\\_E303](#).

### Revision 0.2

January, 2022

- Added [CUR\\_E303](#), [DCDC\\_E302](#) and [USART\\_E304](#).

### Revision 0.1

July, 2021

- Initial release.

# Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!



**IoT Portfolio**  
[www.silabs.com/IoT](http://www.silabs.com/IoT)



**SW/HW**  
[www.silabs.com/simplicity](http://www.silabs.com/simplicity)



**Quality**  
[www.silabs.com/quality](http://www.silabs.com/quality)



**Support & Community**  
[www.silabs.com/community](http://www.silabs.com/community)

## Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

**Note: This content may contain offensive terminology that is now obsolete. Silicon Labs is replacing these terms with inclusive language wherever possible. For more information, visit [www.silabs.com/about-us/inclusive-lexicon-project](http://www.silabs.com/about-us/inclusive-lexicon-project)**

## Trademark Information

Silicon Laboratories Inc., Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Redpine Signals®, WiSeConnect, n-Link, ThreadArch®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, Precision32®, Simplicity Studio®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

[www.silabs.com](http://www.silabs.com)