EFR32BG1 Blue Gecko *Bluetooth*® Smart SoC CSP Family Data Sheet

The Blue Gecko Bluetooth Smart family of SoCs is part of the Wireless Gecko portfolio. Blue Gecko SoCs are ideal for enabling energy-friendly Bluetooth Smart networking for IoT devices.

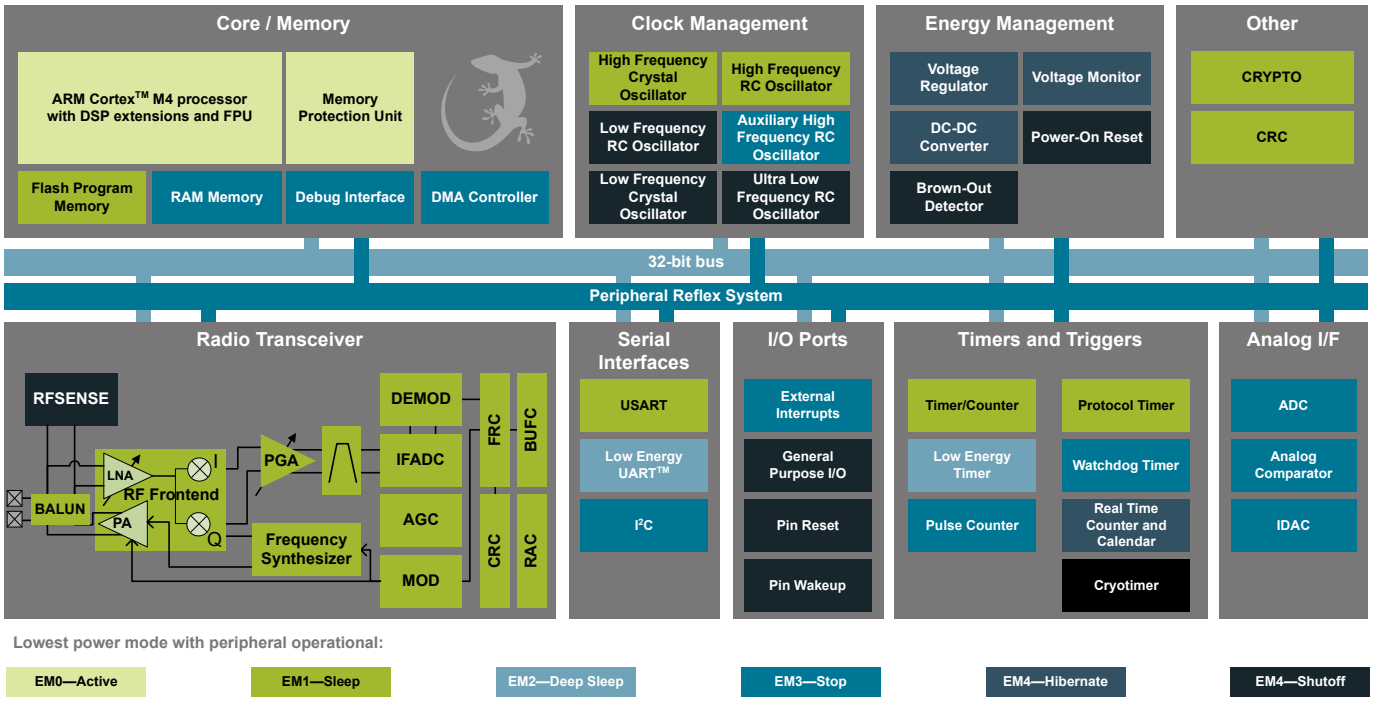
The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, an integrated balun and no-compromise MCU features.

Blue Gecko applications include:

- IoT Sensors and End Devices
- Health and Wellness
- Home and Building Automation
- Accessories
- Human Interface Devices
- Metering
- Commercial and Retail Lighting and Sensing

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- Scalable Memory and Radio configuration options available in footprint-compatible CSP packaging
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated 2.4 GHz balun and PA with up to 19.5 dBm transmit power
- Integrated DC-DC with RF noise mitigation
- Also Available: Certified modules with compatible tools and software



1. Feature List

The EFR32BG1 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 256 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to 19.5 dBm
- **Low Energy Consumption**
  - 8.7 mA RX current at 2.4 GHz
  - 8.2 mA TX current @ 0 dBm output power at 2.4 GHz
  - 63 µA/MHz in Active Mode (EM0)
  - 2.5 µA EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 0.58 µA EM4H Hibernate Mode (128 byte RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -91 dBm sensitivity @ 1 Mbit/s GFSK (2.4GHz)
- **Supported Modulation Format**
  - GFSK
  - 2-FSK / 4-FSK with fully configurable shaping (EFR32BG1P OPNs)
  - Shaped OQPSK / (G)MSK (EFR32BG1P OPNs)
  - Configurable DSSS and FEC (EFR32BG1P OPNs)
- **Supported Protocol:**
  - Bluetooth® Smart
  - Proprietary Protocols (EFR32BG1P OPNs)
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generation
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2× Analog Comparator (ACMP)
  - Digital to Analog Current Converter (IDAC)
  - Up to 19 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
  - Up to 19 General Purpose I/O pins with output state retention and asynchronous interrupts
  - Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator @ 50nA
  - 2×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - Low Energy UART (LEUART™)
  - I^2C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.85 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - -40 °C to 85 °C
- **43-pin CSP 3.3x3.14 mm Package**

2. Ordering Information

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)
EFR32BG1P332F256GJ43-C0	• Bluetooth Smart • Proprietary	2.4 GHz @ 19.5 dBm	256	32
EFR32BG1B232F256GJ43-C0	Bluetooth Smart	2.4 GHz @ 10.5 dBm	256	32
EFR32BG1V132F256GJ43-C0	Bluetooth Smart	2.4 GHz @ 0 dBm	256	16

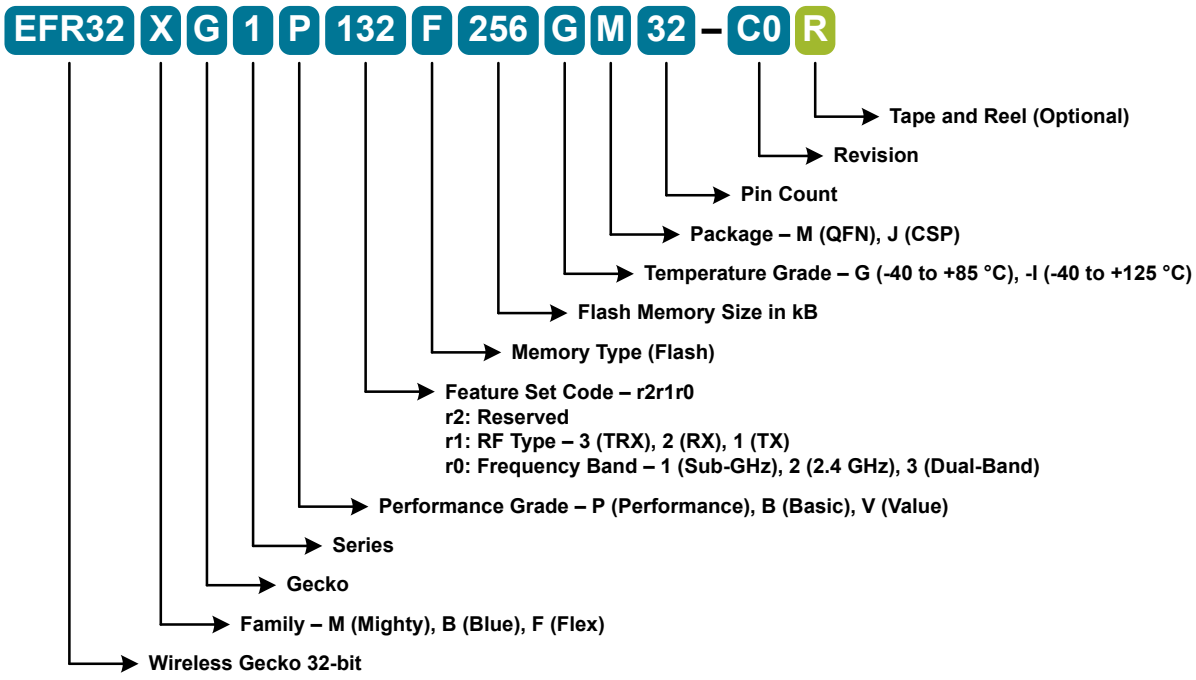


Figure 2.1. OPN Decoder

3. System Overview

3.1 Introduction

The product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the Reference Manual.

A block diagram of the EFR32BG1 family is shown in Figure 3.1 Detailed EFR32BG1 Block Diagram on page 3. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

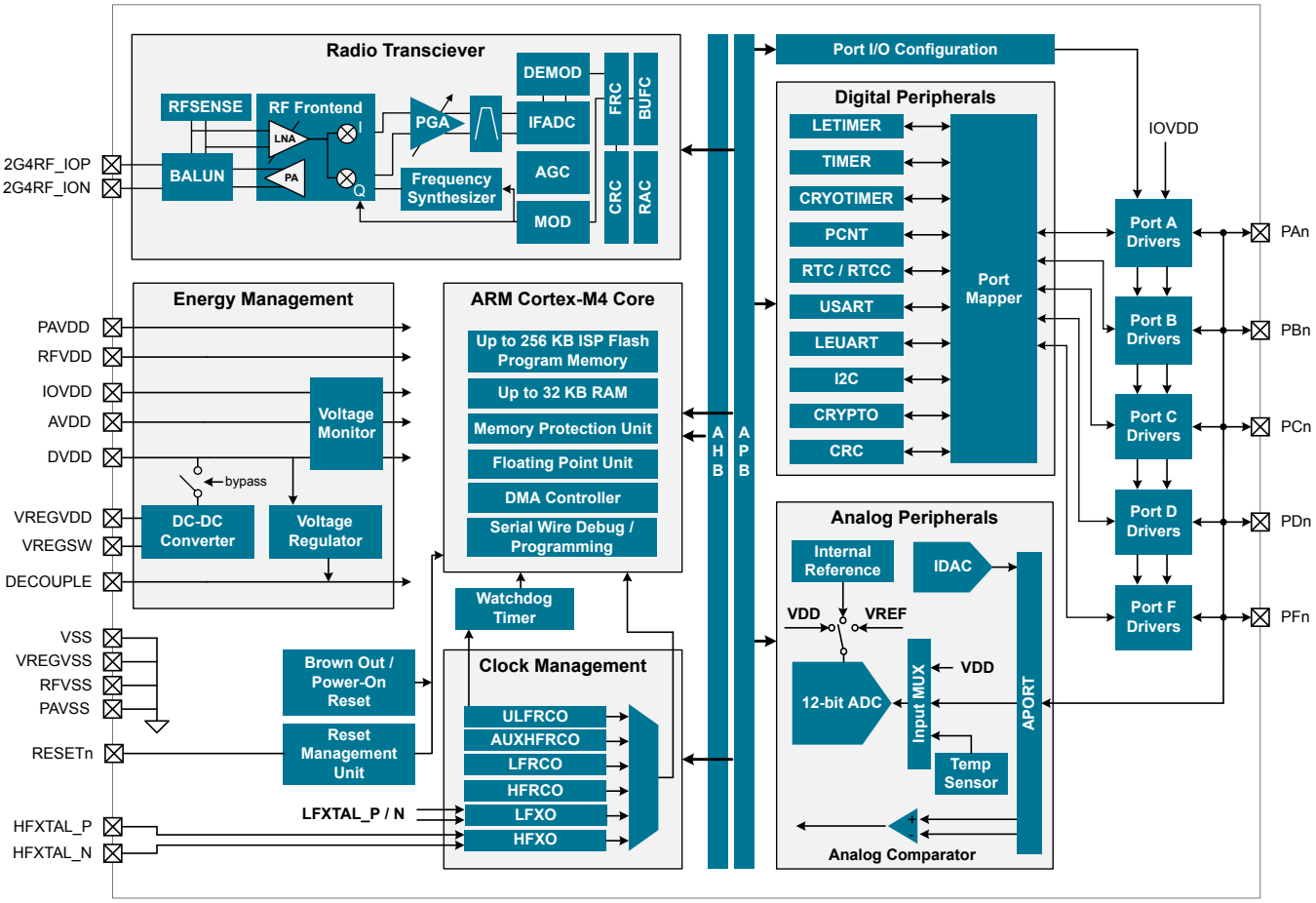


Figure 3.1. Detailed EFR32BG1 Block Diagram

3.2 Radio

The Blue Gecko family features a radio transceiver supporting Bluetooth Smart® and proprietary short range wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32BG1 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.2.3 Receiver Architecture

The EFR32BG1 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. Devices are production-calibrated to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32BG1 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32BG1. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32BG1 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.6 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.7 Flexible Frame Handling

EFR32BG1 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.2.8 Packet and State Trace

The EFR32BG1 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.9 Data Buffering

The EFR32BG1 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32BG1. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The EFR32BG1 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

AVDD and VREGVDD need to be 1.85 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

EFR32BG1 has up to 19 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32BG1. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32BG1 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32BG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32BG1 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

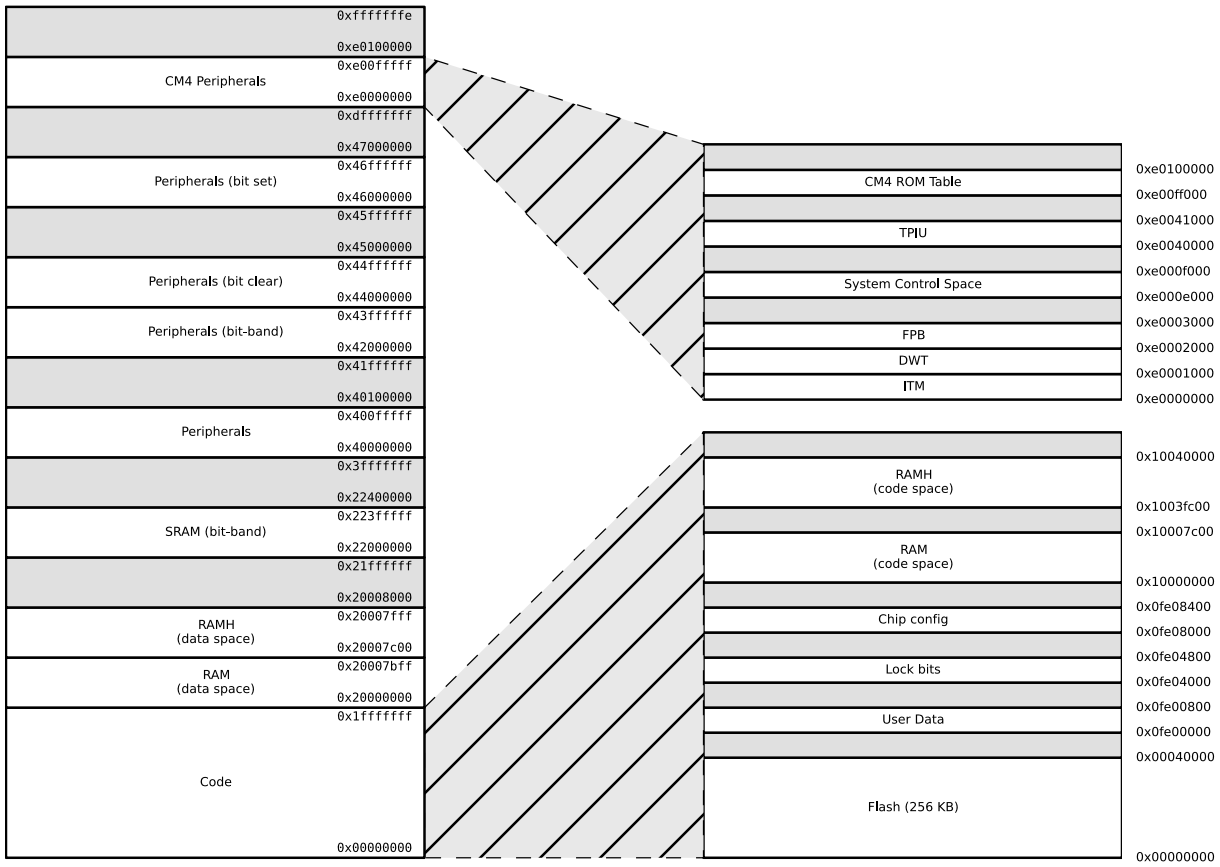


Figure 3.2. EFR32BG1 Memory Map — Core Peripherals and Code Space

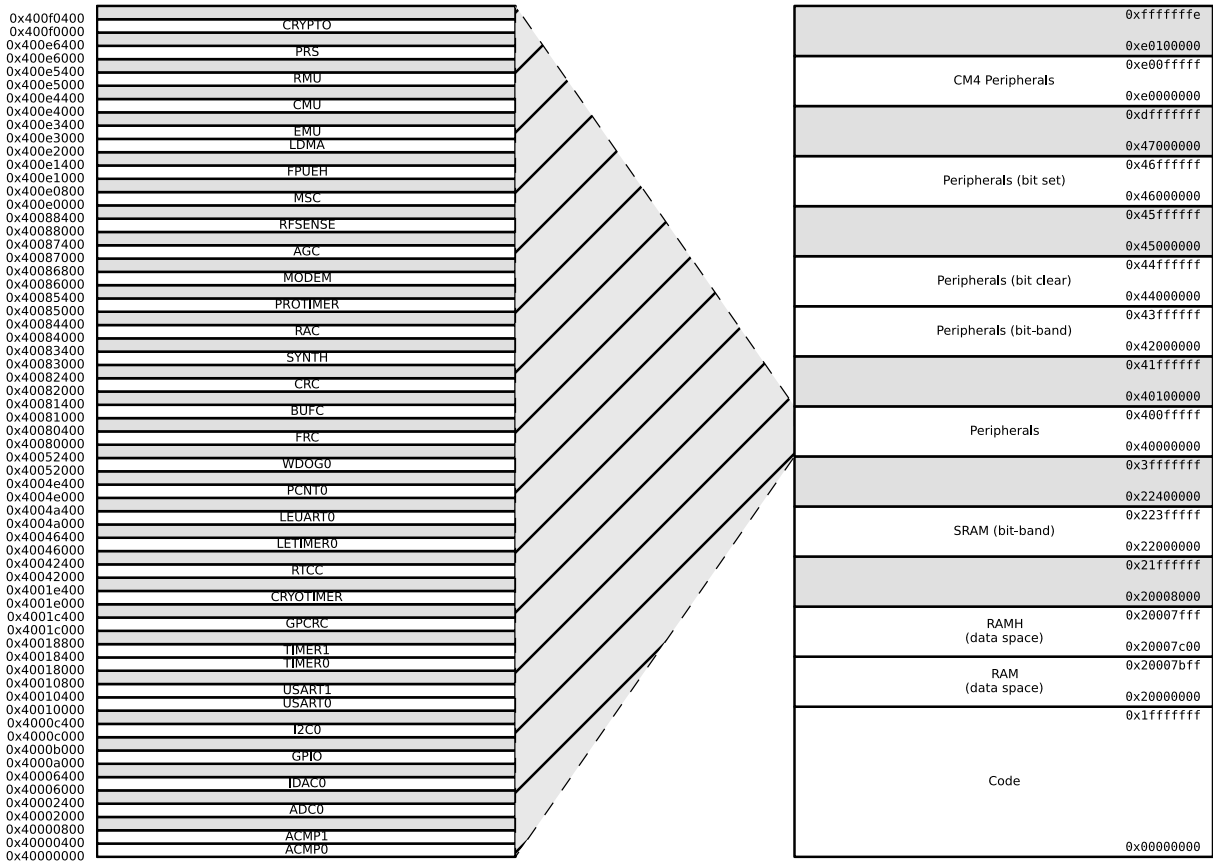


Figure 3.3. EFR32BG1 Memory Map — Peripherals

3.13 Configuration Summary

The features of the EFR32BG1 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI.	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to Table 4.2 General Operating Conditions on page 14 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Input RF level on pins 2G4RF_IOP and 2G4RF_ION	$P_{RFMAX2G4}$		—	—	10	dBm
Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION)	$V_{MAXDIFF2G4}$		-50	—	50	mV
Absolute Voltage on RF pins 2G4RF_IOP and 2G4RF_ION	V_{MAX2G4}		-0.3	—	3.3	V
Total current into VDD power lines (source)	I_{VDDMAX}		—	—	200	mA
Total current into VSS ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		—	—	0.3	V
Junction Temperature	T_J		-40	—	105	°C

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highest voltage in the system
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD
- PAVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	-G temperature grade, Ambient Temperature	-40	25	85	°C
AVDD Supply voltage[1]	V_{AVDD}		1.85	3.3	3.8	V
VREGVDD Operating supply voltage[1 2]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.85	3.3	3.8	V
VREGVDD Current	$I_{VREGVDD}$	DCDC in bypass	—	—	200	mA
RFVDD Operating supply voltage	V_{RFVDD}		1.62	—	$V_{VREGVDD}$	V
DVDD Operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
PAVDD Operating supply voltage	V_{PAVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD Operating supply voltage	V_{IOVDD}		1.62	—	$V_{VREGVDD}$	V
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)	dV_{DD}		—	—	0.1	V
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [3]	—	—	26	MHz
		1 wait-states (MODE = WS1) [3]	—	—	40	MHz

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$
3. In MSC_READCTRL register

4.1.3 DC-DC Converter

Test conditions: L_{DCDC}=4.7 µH (Murata LQH3NPN4R7MM0L), C_{DCDC}=1.0 µF (Murata GRM188R71A105KA61D), V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, I_{DCDC_LOAD}=50 mA, Heavy Drive configuration, F_{DCDC_LN}=7 MHz, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.85	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC Accuracy	ACC_{DC}	Low noise (LN) mode, 1.8 V target output	1.7	—	1.9	V
Regulation Window[2]	WIN_{REG}	Low power (LP) mode, LPCMPBIAS[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	1.63	—	2.2	V
		Low power (LP) mode, LPCMPBIAS[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	1.63	—	2.1	V
Steady-state output ripple	V_R	Radio disabled.	—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	—	150	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	—	150	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	50	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	125	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[4]	—	—	200	mA
		Low noise (LN) mode, Medium Drive[4]	—	—	100	mA
		Low noise (LN) mode, Light Drive[4]	—	—	50	mA
		Low power (LP) mode, LPCMPBIAS[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIAS[3] = 3	—	—	10	mA
DCDC nominal output capacitor	C_{DCDC}	25% tolerance	1	1	1	µF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R_{BYP}		—	1.2	2.5	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits
3. In EMU_DCDCMISCCTRL register
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 3.3 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See Figure 5.1 EFR32BG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter on page 64.

Table 4.4. Current Consumption 3.3V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	130	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	105	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	106	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	222	350	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	65	—	µA/MHz
		38 MHz HFRCO	—	35	38	µA/MHz
		26 MHz HFRCO	—	37	41	µA/MHz
		1 MHz HFRCO	—	157	275	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.3	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	3	6.3	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.8	6	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.1	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.65	—	µA
		128 byte RAM retention, no RTCC	—	0.65	1.3	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	0.11	µA

Note:
1. CMU_HFXOCTRL_LOWPOWER=0

4.1.4.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD = 1.8 V DC-DC output. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64.

Table 4.5. Current Consumption 3.3V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode[1].	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[2]	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	71	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	µA/MHz
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode[3].		38.4 MHz crystal, CPU running while loop from flash[2]	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	75	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	88	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode[1].	I_{EM1}	38.4 MHz crystal[2]	—	49	—	µA/MHz
		38 MHz HFRCO	—	32	—	µA/MHz
		26 MHz HFRCO	—	38	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode[3].		38.4 MHz crystal[2]	—	61	—	µA/MHz
		38 MHz HFRCO	—	45	—	µA/MHz
		26 MHz HFRCO	—	58	—	µA/MHz
Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode[4].	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	2.5	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	2.3	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.1	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	0.86	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.58	—	µA
		128 byte RAM retention, no RTCC	—	0.58	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD
2. CMU_HFXOCTRL_LOWPOWER=0
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DVDD

4.1.4.3 Current Consumption 1.85 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 1.85 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See Figure 5.1 EFR32BG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter on page 64.

Table 4.6. Current Consumption 1.85V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	131	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	220	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	65	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	154	—	µA/MHz
Current consumption in EM2 Deep Sleep mode	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.2	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	2.8	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.7	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.62	—	µA
		128 byte RAM retention, no RTCC	—	0.62	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	No RAM retention, no RTCC	—	0.02	—	µA

Note:
1. CMU_HFXOCTRL_LOWPOWER=0

4.1.4.4 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 or Figure 5.1 EFR32BG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter on page 64.

Table 4.7. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{RX}	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	8.7	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{TX}	F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3	—	8.2	—	mA
		F = 2.4 GHz, CW, 3 dBm output power	—	16.5	—	mA
		F = 2.4 GHz, CW, 8 dBm output power	—	23.3	—	mA
		F = 2.4 GHz, CW, 10.5 dBm output power	—	32.7	—	mA
		F = 2.4 GHz, CW, 16.5 dBm output power, PAVDD connected directly to external 3.3V supply	—	83.9	—	mA
		F = 2.4 GHz, CW, 19.5 dBm output power, PAVDD connected directly to external 3.3V supply	—	126.7	—	mA
RFSENSE current consumption	$I_{RFSENSE}$		—	51	—	nA

4.1.5 Wake up times

Table 4.8. Wake up times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep Sleep	t_{EM2_WU}	Code execution from flash	—	10.7	—	µs
		Code execution from RAM	—	3	—	µs
Wakeup time from EM1 Sleep	t_{EM1_WU}	Executing from flash	—	3	—	AHB Clocks
		Executing from RAM	—	3	—	AHB Clocks
Wake up from EM3 Stop	t_{EM3_WU}	Executing from flash	—	10.7	—	µs
		Executing from RAM	—	3	—	µs
Wake up from EM4H Hibernate[1]	t_{EM4H_WU}	Executing from flash	—	60	—	µs
Wake up from EM4S Shutoff[1]	t_{EM4S_WU}		—	290	—	µs

Note:
1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

4.1.6 Brown Out Detector

Table 4.9. Brown Out Detector

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDDBOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling	1.35	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	24	—	mV
DVDD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.85	V
		AVDD falling	1.62	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	21	—	mV
AVDD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	46	—	mV
EM4 response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.7 Frequency Synthesizer Characteristics

Table 4.10. Frequency Synthesizer Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F_{RANGE_2400}	2.4 GHz frequency range	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	F_{RES_2400}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	ΔF_{MAX_2400}		—	—	1677	kHz

4.1.8 2.4 GHz RF Transceiver Characteristics

4.1.8.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz. Test circuit according to Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65.

Table 4.11. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power[1]	$POUT_{MAX}$	19.5 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply[2]	—	19.5	—	dBm
		10.5 dBm-rated part numbers	—	10.5	—	dBm
		0 dBm-rated part numbers	—	0	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-30	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm< Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.85 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power > 10.5 dBm.	—	4.5	—	dB
		1.85 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power = 10.5 dBm.	—	3.8	—	dB
		1.85 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter	—	2.2	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85 °C, PAVDD connected to DC-DC output	—	1.5	—	dB
		From -40 to +85 °C, PAVDD connected to external supply	—	1.5	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range	—	0.4	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of 2. Ordering Information
2. For Bluetooth, the Maximum TX power on Channel 2456 is limited to +15 dBm to comply with In-band Spurious emissions.

4.1.8.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65.

Table 4.12. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm
Level above which RFSENSE will trigger[1]	$RFSENSE_{TRIG}$	CW at 2.45 GHz	—	-24	—	dBm
Level below which RFSENSE will not trigger[1]	$RFSENSE_{THRES}$		—	-50	—	dBm
1% PER Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal[2]	—	-89.2	—	dBm
0.1% BER Sensitivity		250 kbps 2GFSK signal	—	-99.1	—	dBm

Note:

1. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.
2. Channel at 2420 MHz will have degraded sensitivity. Sensitivity could be as high as -83dBm on this channel.

4.1.8.3 RF Transmitter Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.44 GHz. Test circuit according to Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65.

Table 4.13. RF Transmitter Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6dB bandwidth	TXBW		—	740	—	kHz
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247 at 10 dBm	—	-6.5	—	dBm/ 3kHz
		Per FCC part 15.247 at 20 dBm	—	-2.6	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	10	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions at 10 dBm, with allowed exceptions[1]	$SPUR_{INB}$	At ±2 MHz	—	-39.8	—	dBm
		At ±3 MHz	—	-42.1	—	dBm
In-band spurious emissions at 20 dBm, with allowed exceptions[1] [2]		At ±2 MHz	—	—	-20	dBm
		At ±3 MHz	—	—	-30	dBm
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM\_FCC}$	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	—	-47	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$. Restricted Bands	$SPUR_{OOB\_FCC}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier[3]	—	-47	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$. Non Restricted Bands		Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328	$SPUR_{ETSI328}$	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz	—	-42	—	dBm
		1-12 GHz	—	-36	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Per Bluetooth Core_4.2, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2456 MHz, a maximum output power of 15 dBm is used to achieve this value.
3. For 2480 MHz, a maximum duty cycle of 20% is used to achieve this value.

4.1.8.4 RF Receiver Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65.

Table 4.14. RF Receiver Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER[2]	SENS	Signal is reference signal[1]. Using DC-DC converter	—	-91	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1	—	-90.2	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity	—	8.3	—	dB
N+1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-3.3	—	dB
N-1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	1.3	—	dB
Alternate (2 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-39.5	—	dB
Alternate (3 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_3	Interferer is reference signal at ±3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-43.8	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-29	—	dB
Selectivity to image frequency +1 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision	—	-43.6	—	dB
Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range.	$BLOCK_{OOB}$	Interferer frequency 30 MHz ≤ f ≤ 2000 MHz	—	-27	—	dBm
		Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz	—	-32	—	dBm
		Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz	—	-32	—	dBm
		Interferer frequency 3 GHz ≤ f ≤ 12.75 GHz	—	-27	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermodulation performance	IM	Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3	—	-25.8	—	dBm
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		4	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		—	—	-101	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	—	0.5	dB

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm
2. Receive sensitivity on Bluetooth Smart channel 26 is -86 dBm

4.1.8.5 RF Transmitter Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T=25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Test circuit according to Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65.

Table 4.15. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude (offset EVM), per 802.15.4-2011, not including 2415 MHz channel[1]	EVM	Average across frequency. Signal is DSSS-OQPSK reference packet[2]	—	5.5	—	% rms
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ±3.5 MHz	—	-26	—	dBc
		Absolute, at carrier ±3.5 MHz[3]	—	-36	—	dBm
		Per FCC part 15.247	—	-4.2	—	dBm/ 3kHz
		Output power level which meets 10dBm/MHz ETSI 300.328 specification	—	12	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	—	2.25	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier	—	-45.8	—	dBm
Spurious emissions of harmonics in harmonics in non-restricted bands per FCC Part 15.247/15.35, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz	$SPUR_{HRM\_FCC\_NRR}$		—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in restricted bands (30-88 MHz), per FCC part 15.205/15.209, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz	$SPUR_{OOB\_FCC\_R}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier[4]	—	-52	—	dBm
Spurious emissions out-of-band in restricted bands (88-216 MHz), per FCC part 15.205/15.209, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz			—	-62	—	dBm
Spurious emissions out-of-band in restricted bands (216-960 MHz), per FCC part 15.205/15.209, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz			—	-57	—	dBm
Spurious emissions out-of-band in restricted bands (>960 MHz), per FCC part 15.205/15.209, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz			—	-48	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247, Emissions taken at Pout_Max power level of 19.5 dBm, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz	$SPUR_{OOB\_FCC\_NR}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328[5]	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW];	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW]; per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440[5]	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies	—	-42	—	dBm
		1G-14G	—	-36	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Typical EVM for the 2415 MHz channel is 7.9%
2. Reference packet is defined as 20 octet PSDU, modulated according to 802.15.4-2011 DSSS-OQPSK in the 2.4GHz band, with pseudo-random packet data content
3. For 2415 MHz, a maximum duty cycle of 50% is used to achieve this value.
4. For 2480 MHz, a maximum duty cycle of 20% is used to achieve this value.
5. Specified at maximum power output level of 10 dBm

4.1.8.6 RF Receiver Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T=25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.445 GHz. Test circuit according to Figure 5.2 EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC) on page 64 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65.

Table 4.16. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal[1]. Packet length is 20 octets.	—	10	—	dBm
Sensitivity, 1% PER[2]	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	—	-101	—	dBm
		Signal is reference signal. Packet length is 20 octets. Without DC-DC converter.	—	-101	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 10 dB above sensitivity limit	—	-2.6	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[3]	ACR_{+1}	Interferer is reference signal at +1 channel-spacing.	—	33.75	—	dB
		Interferer is filtered reference signal[4] at +1 channel-spacing.	—	52.2	—	dB
		Interferer is CW at +1 channel-spacing.[5]	—	58.6	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[3]	ACR_{-1}	Interferer is reference signal at -1 channel-spacing.	—	35	—	dB
		Interferer is filtered reference signal[4] at -1 channel-spacing.	—	54.7	—	dB
		Interferer is CW at -1 channel-spacing.	—	60.1	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[3]	ACR_2	Interferer is reference signal at ±2 channel-spacing	—	45.9	—	dB
		Interferer is filtered reference signal[4] at ±2 channel-spacing	—	56.8	—	dB
		Interferer is CW at ±2 channel-spacing	—	65.5	—	dB
Image rejection, 1% PER, Desired is reference signal at 3dB above reference sensitivity level[3]	IR	Interferer is CW in image band[5]	—	40.8	—	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level[3]. Interferer is reference signal.	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	57.2	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	57.9	—	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz	$BLOCK_{80211G}$	Desired is reference signal at 6dB above reference sensitivity level[3]	—	51.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		5	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		—	—	-98	dBm
RSSI resolution	$RSSI_{RES}$	over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2003	$RSSI_{LIN}$		—	±1	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s
2. Receive sensitivity on 802.15.4 channel 14 is -98 dBm
3. Reference sensitivity level is -85 dBm
4. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stopband rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
5. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ±5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.1.9 Modem Features

Table 4.17. Modem Features

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Bandwidth	$RX_{Bandwidth}$	Configurable range with 38.4 MHz crystal	0.1	—	2530	kHz
IF Frequency	IF_{Freq}	Configurable range with 38.4 MHz crystal. Selected steps available.	150	—	1371	kHz

4.1.10 Oscillators

4.1.10.1 LFXO

Table 4.18. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kΩ, C_L = 7 pF, GAIN[4] = 3, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR=70 kΩ, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register
4. In CMU_LFXOCTRL register

4.1.10.2 HFXO

Table 4.19. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	9	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ω, C_L = 10 pF	—	300	—	µs
Frequency Tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ω, CL = 10 pF	-40	—	40	ppm

Note:
1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.10.3 LFRCO

Table 4.20. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	26.2	32.768	34.5	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	26.2	32.768	34.5	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register

4.1.10.4 HFRCO and AUXHFRCO

Table 4.21. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	f_{HFRCO_ACC}	Any frequency band, across supply voltage and temperature	-10	—	3	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	$f_{HFRCO} = 38$ MHz	—	204	228	µA
		$f_{HFRCO} = 32$ MHz	—	171	190	µA
		$f_{HFRCO} = 26$ MHz	—	147	164	µA
		$f_{HFRCO} = 19$ MHz	—	126	138	µA
		$f_{HFRCO} = 16$ MHz	—	110	120	µA
		$f_{HFRCO} = 13$ MHz	—	100	110	µA
		$f_{HFRCO} = 7$ MHz	—	81	91	µA
		$f_{HFRCO} = 4$ MHz	—	33	35	µA
		$f_{HFRCO} = 2$ MHz	—	31	35	µA
		$f_{HFRCO} = 1$ MHz	—	30	35	µA
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.10.5 ULFRCO

Table 4.22. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.8	1	1.05	kHz

4.1.11 Flash Memory Characteristics

Table 4.23. Flash Memory Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}		10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	26	40	µs
Page erase time	t_{PERASE}		20	27	40	ms
Mass erase time	t_{MERASE}		20	27	40	ms
Device erase time[2]	t_{DERASE}		—	60	74	ms
Page erase current[3]	I_{ERASE}		—	—	3	mA
Mass or Device erase current[3]			—	—	5	mA
Write current[3]	I_{WRITE}		—	—	3	mA

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
3. Measured at 25°C

4.1.12 GPIO

Table 4.24. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	IOVDD*0.3	V
Input high voltage	V_{IOIH}		IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{IOOH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{IOOL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD	—	0.1	30	nA
		LFXO Pins, GPIO ≤ IOVDD	—	0.1	50	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up resistor	R_{PU}		30	43	65	kΩ
I/O pin pull-down resistor	R_{PD}		30	43	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		20	25	35	ns
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register

4.1.13 VMON

Table 4.25. VMON

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VMON Supply Current	I_{VMON}	In EM0 or EM1, 1 supply monitored	—	5.8	8.26	µA
		In EM0 or EM1, 4 supplies monitored	—	11.8	16.8	µA
		In EM2, EM3 or EM4, 1 supply monitored	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored	—	99	—	nA
VMON Loading of Monitored Supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.14 ADC

Table 4.26. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range	V_{ADCIN}	Single ended	0	—	$2*V_{REF}$	V
		Differential	$-V_{REF}$	—	V_{REF}	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[1]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	301	350	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	149	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	91	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	51	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	9	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	117	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	79	—	µA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	345	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	191	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	132	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	102	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	17	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	162	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	123	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	µA
ADC Clock Frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[4]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[2] = NORMAL	—	—	5	µs
		WARMUPMODE[2] = KEEPINSTANDBY	—	—	2	µs
		WARMUPMODE[2] = KEEPINSLOWACC	—	—	1	µs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	58	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	—	380	—	µV
Offset Error	$V_{ADCOFFSETERR}$		-3	0.25	3	LSB
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	—	-0.2	5	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No Missing Codes	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Temperature Sensor Slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL
2. In ADCn_CNTL register
3. In ADCn_BIASPROG register
4. Derived from ADCCLK

4.1.15 IDAC

Table 4.27. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N_{IDAC_RANGES}		—	4	—	-
Output Current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total Accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-5	—	2	%
		EM0 or EM1	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption in EM0 or EM1 [2]	I_{IDAC}	Source mode, excluding output current	—	8.9	13	µA
		Sink mode, excluding output current	—	12	16	µA
Current consumption in EM2 or EM3[2]		Source mode, excluding output current, duty cycle mode, T = 25 °C	—	1.04	—	µA
		Sink mode, excluding output current, duty cycle mode, T = 25 °C	—	1.08	—	µA
		Source mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	8.9	—	µA
		Sink mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.04	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.02	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.02	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.02	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.18	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.08	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.02	—	%

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.16 Analog Comparator (ACMP)

Table 4.28. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL [1]	0	—	$V_{ACMPVDD}$	V
Supply Voltage	$V_{ACMPVDD}$	BIASPROG[2] ≤ 0x10 or FULLBIAS[2] = 0	1.85	—	$V_{VREGVDD\_MAX}$	V
		0x10 < BIASPROG[2] ≤ 0x20 and FULLBIAS[2] = 1	2.1	—	$V_{VREGVDD\_MAX}$	V
Active current not including voltage reference	I_{ACMP}	BIASPROG[2] = 1, FULLBIAS[2] = 0	—	50	—	nA
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	306	—	nA
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	74	95	µA
Current consumption of internal voltage reference	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA
Hysteresis (V_{CM} = 1.25 V, BIASPROG[2] = 0x10, FULLBIAS[2] = 1)	$V_{ACMPHYST}$	HYSTSEL[3] = HYST0	-1.75	0	1.75	mV
		HYSTSEL[3] = HYST1	10	18	26	mV
		HYSTSEL[3] = HYST2	21	32	46	mV
		HYSTSEL[3] = HYST3	27	44	63	mV
		HYSTSEL[3] = HYST4	32	55	80	mV
		HYSTSEL[3] = HYST5	38	65	100	mV
		HYSTSEL[3] = HYST6	43	77	121	mV
		HYSTSEL[3] = HYST7	47	86	148	mV
		HYSTSEL[3] = HYST8	-4	0	4	mV
		HYSTSEL[3] = HYST9	-27	-18	-10	mV
		HYSTSEL[3] = HYST10	-47	-32	-18	mV
		HYSTSEL[3] = HYST11	-64	-43	-27	mV
		HYSTSEL[3] = HYST12	-78	-54	-32	mV
		HYSTSEL[3] = HYST13	-93	-64	-37	mV
		HYSTSEL[3] = HYST14	-113	-74	-42	mV
		HYSTSEL[3] = HYST15	-135	-85	-47	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparator delay[4]	$t_{ACMPDELAY}$	BIASPROG[2] = 1, FULLBIAS[2] = 0	—	30	—	µs
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	3.7	—	µs
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[2] =0x10, FULLBIAS[2] = 1	-35	—	35	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	2	2.5	2.8	V
Capacitive Sense Internal Resistance	R_{CSRES}	CSRESSEL[5] = 0	—	inf	—	kΩ
		CSRESSEL[5] = 1	—	15	—	kΩ
		CSRESSEL[5] = 2	—	27	—	kΩ
		CSRESSEL[5] = 3	—	39	—	kΩ
		CSRESSEL[5] = 4	—	51	—	kΩ
		CSRESSEL[5] = 5	—	102	—	kΩ
		CSRESSEL[5] = 6	—	164	—	kΩ
		CSRESSEL[5] = 7	—	239	—	kΩ

Note:
1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD
2. In ACMPn_CTRL register
3. In ACMPn_HYSTERESIS register
4. ±100 mV differential drive
5. In ACMPn_INPUTSEL register

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

$I_{ACMPREF}$ is zero if an external voltage reference is used.

4.1.17 I2C

I2C Standard-mode (Sm)

Table 4.29. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	$t_{SU,DAT}$		250	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	3450	ns
Repeated START condition set-up time	$t_{SU,STA}$		4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		4	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode (Fm)

Table 4.30. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$		100	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	900	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:
1. For CLHR set to 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode Plus (Fm+)

Table 4.31. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$		50	—	—	ns
SDA hold time	$t_{HD,DAT}$		100	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.18 USART SPI

SPI Master Timing

Table 4.32. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		0	—	8	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		3	—	20	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.62 V	56	—	—	ns
		IOVDD = 3.0 V	37	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		6	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

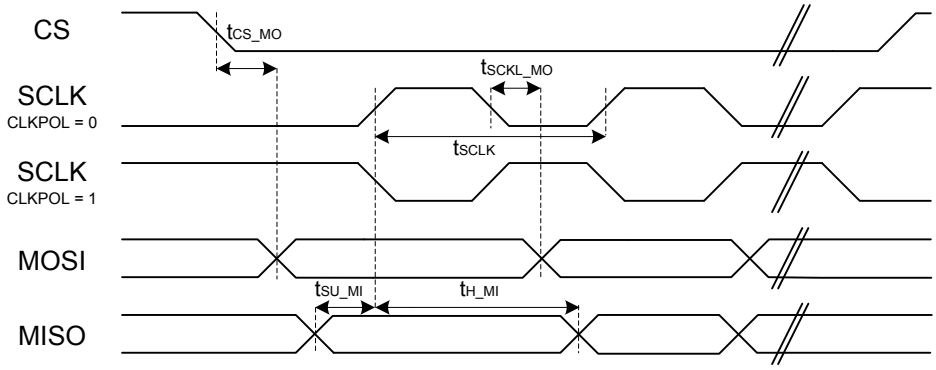


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.33. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCKL period [1] [2]	t_{SCLK_sl}		2 * $t_{HFPERCLK}$	—	—	ns
SCLK high period[1] [2]	t_{SCLK_hi}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low period [1] [2]	t_{SCLK_lo}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1] [2]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1] [2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

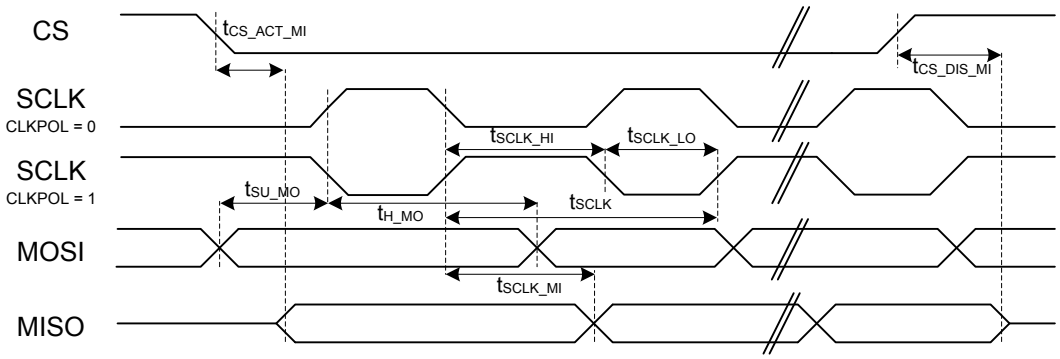


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

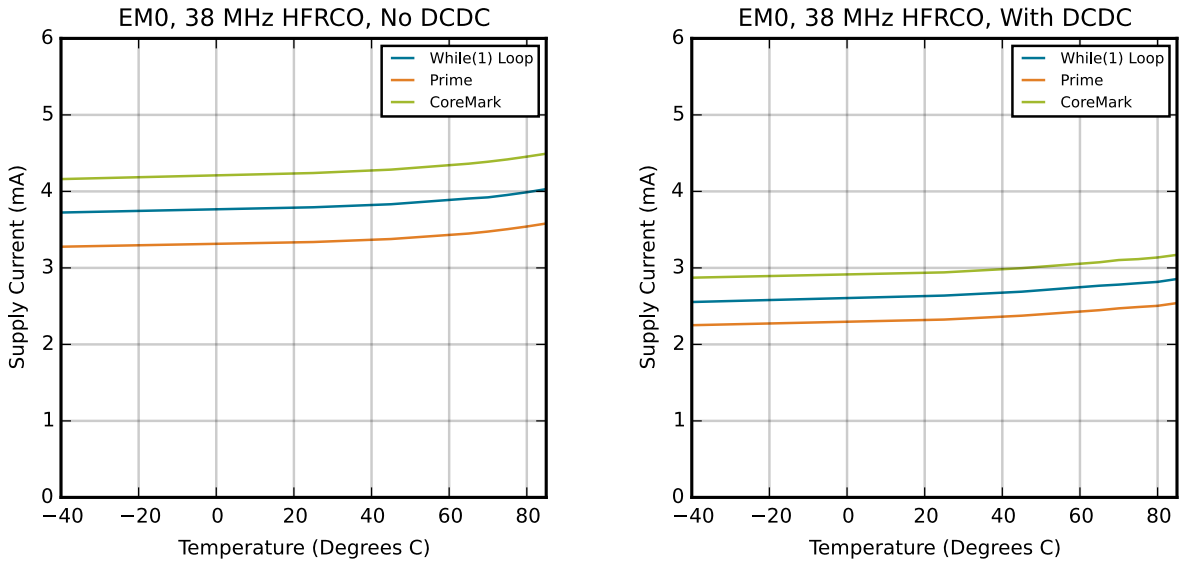


Figure 4.3. EM0 Active Mode Typical Supply Current

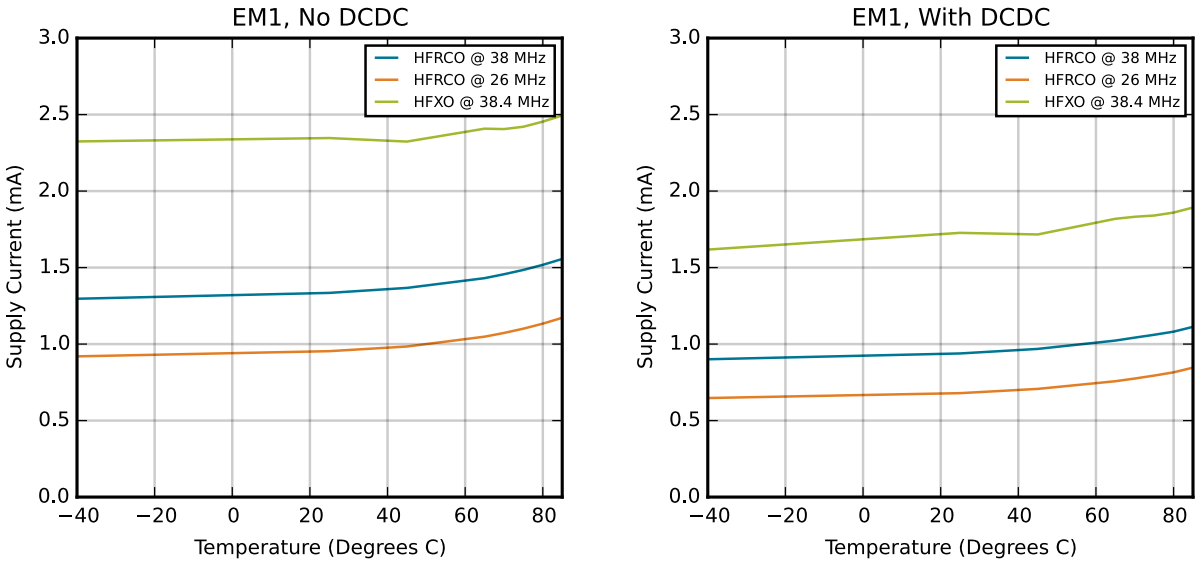


Figure 4.4. EM1 Sleep Mode Typical Supply Current

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

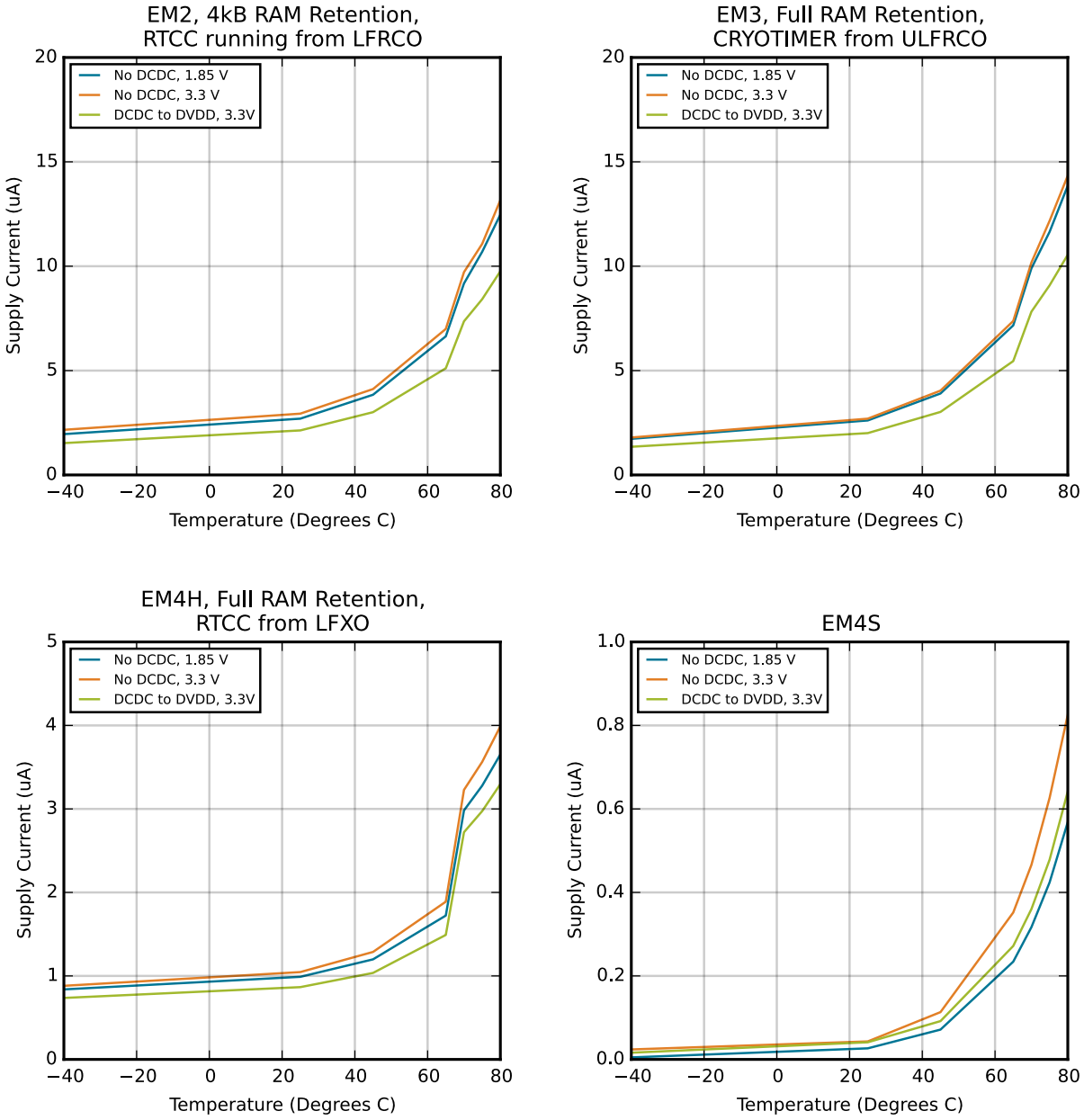


Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 1.0 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

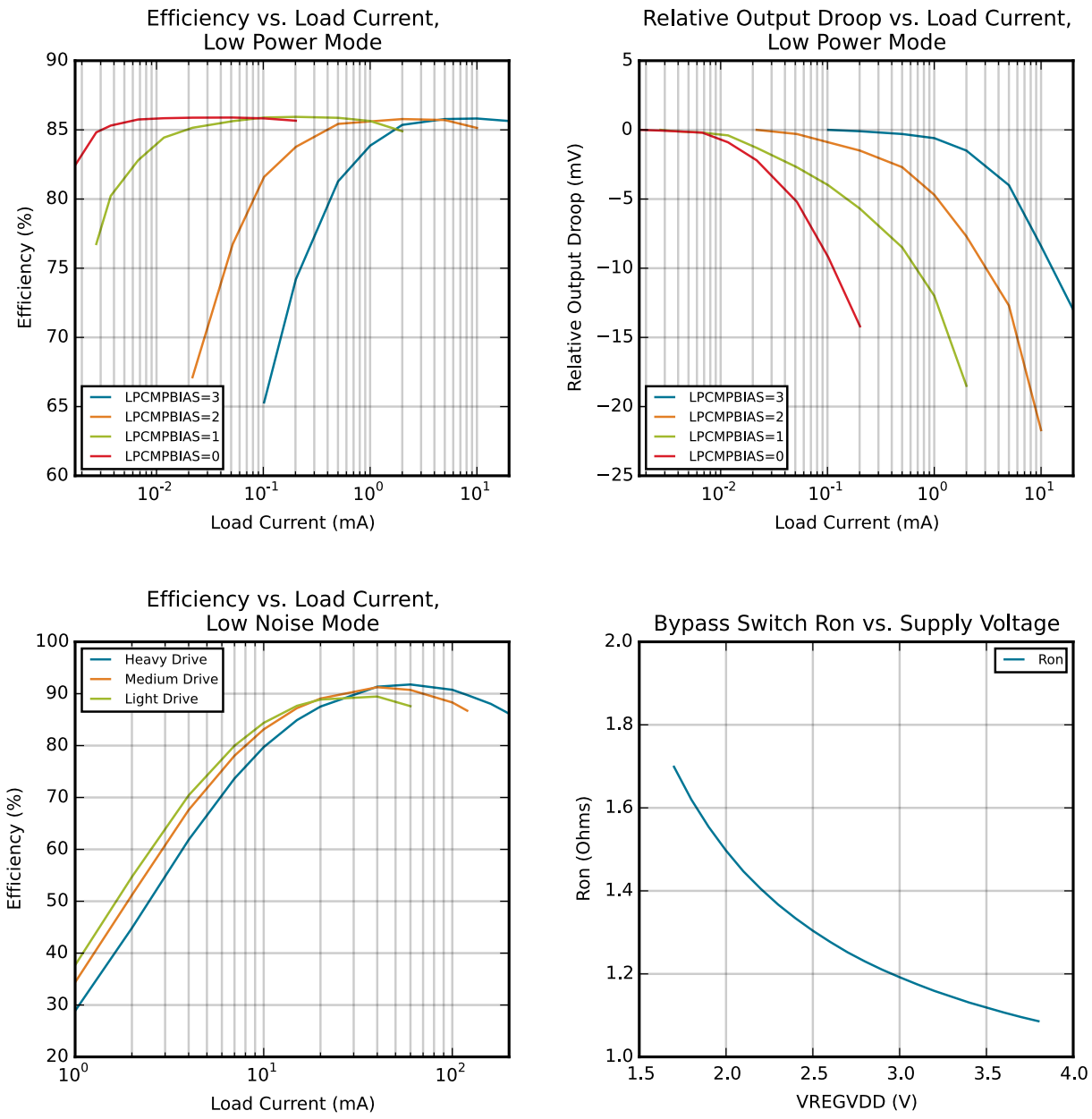


Figure 4.6. DC-DC Converter Typical Performance Characteristics

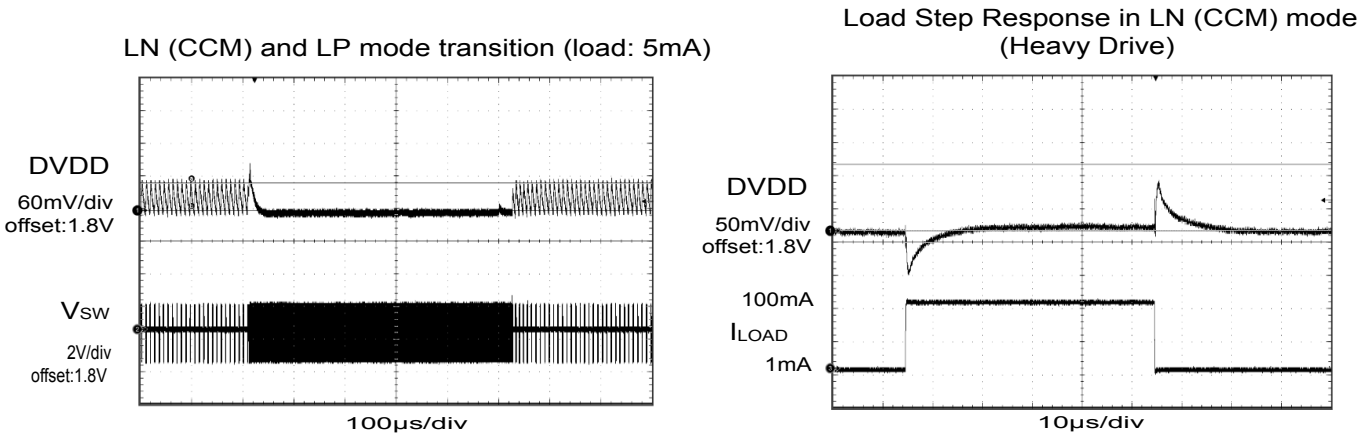


Figure 4.7. DC-DC Converter Transition Waveforms

4.2.3 Internal Oscillators

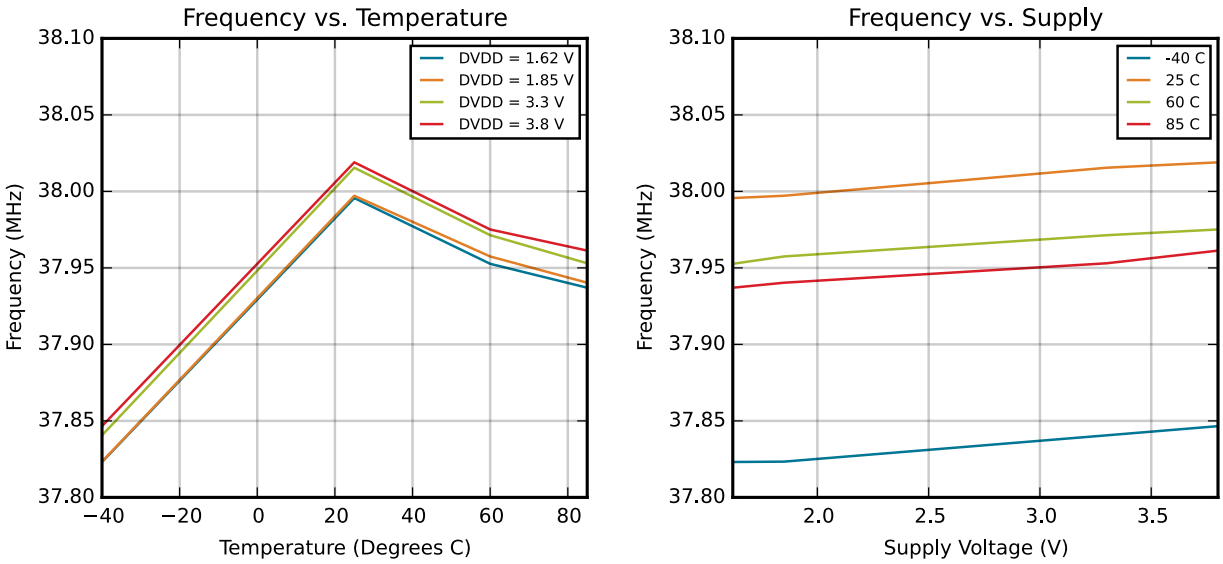


Figure 4.8. HFRCO and AUXHFRCO Typical Performance at 38 MHz

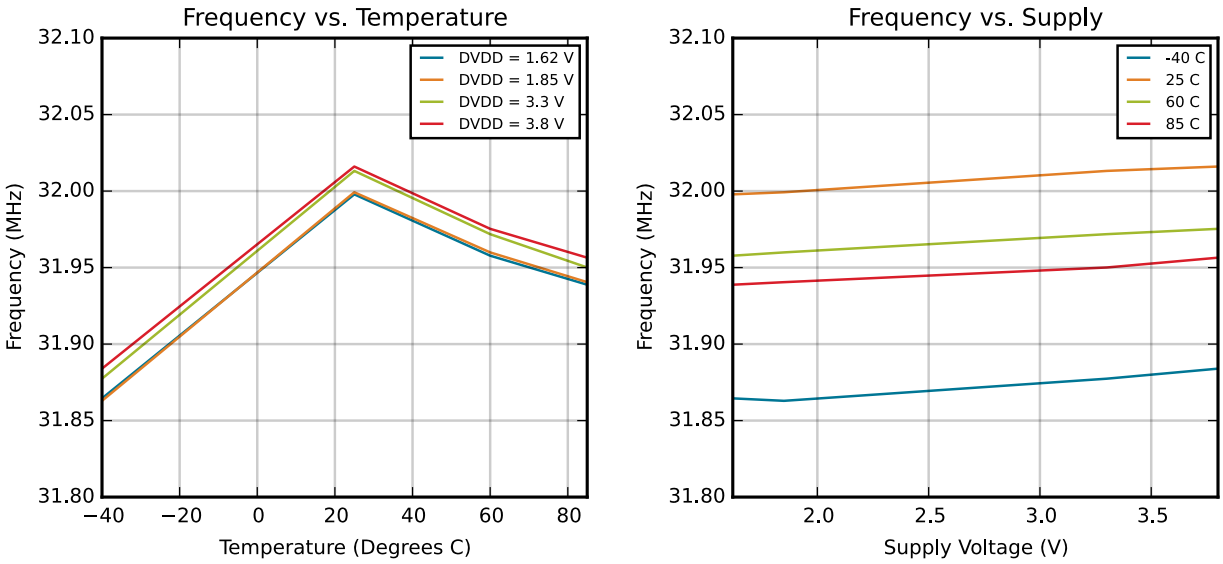


Figure 4.9. HFRCO and AUXHFRCO Typical Performance at 32 MHz

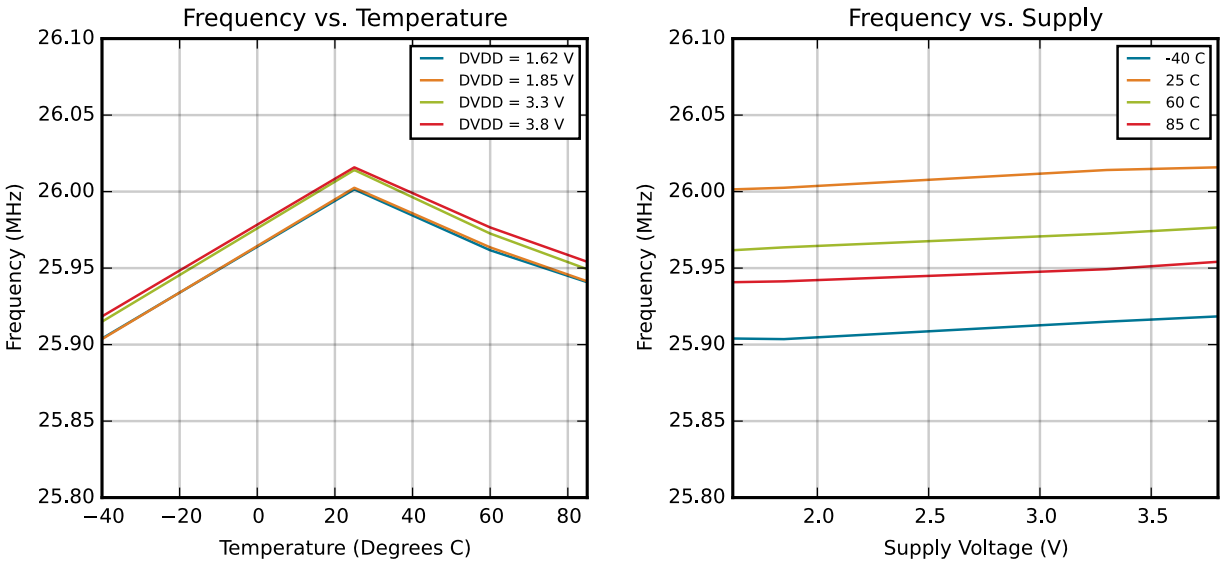


Figure 4.10. HFRCO and AUXHFRCO Typical Performance at 26 MHz

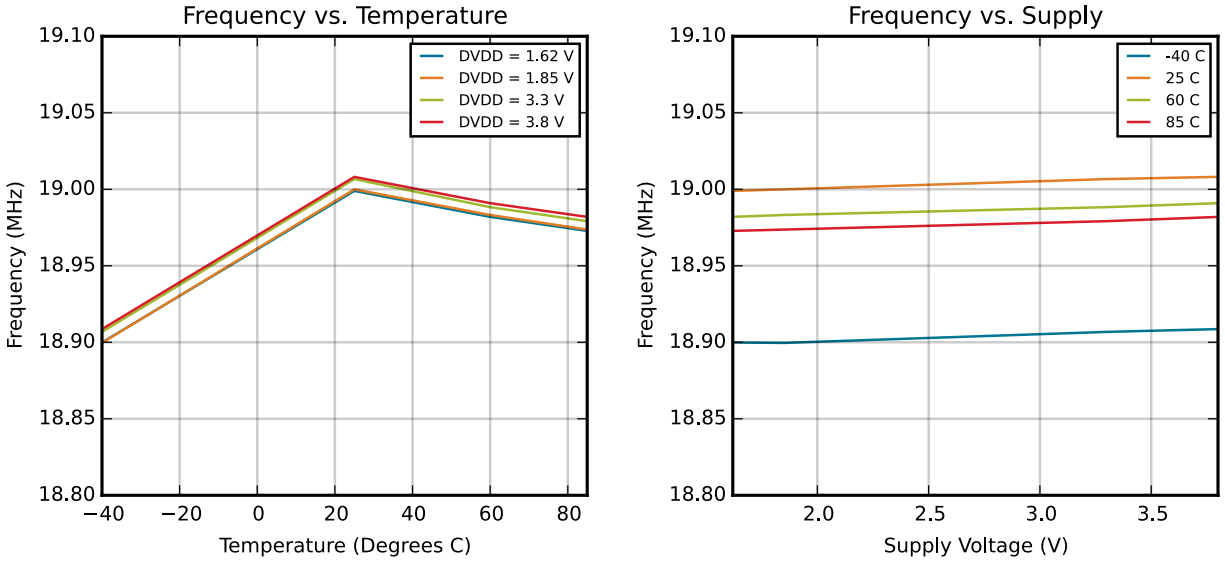


Figure 4.11. HFRCO and AUXHFRCO Typical Performance at 19 MHz

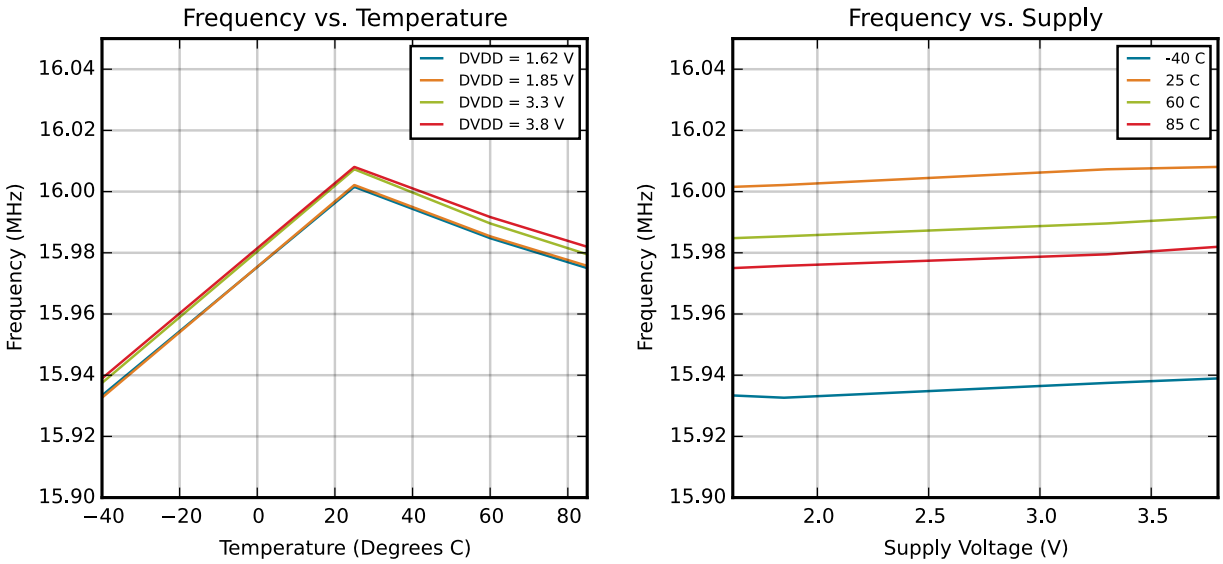


Figure 4.12. HFRCO and AUXHFRCO Typical Performance at 16 MHz

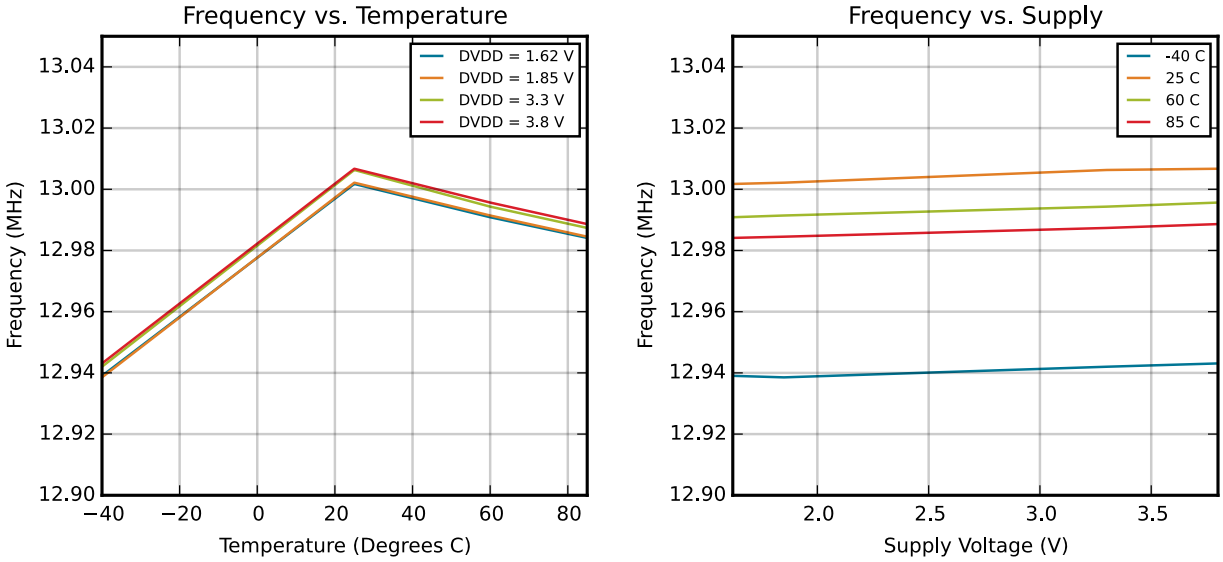


Figure 4.13. HFRCO and AUXHFRCO Typical Performance at 13 MHz

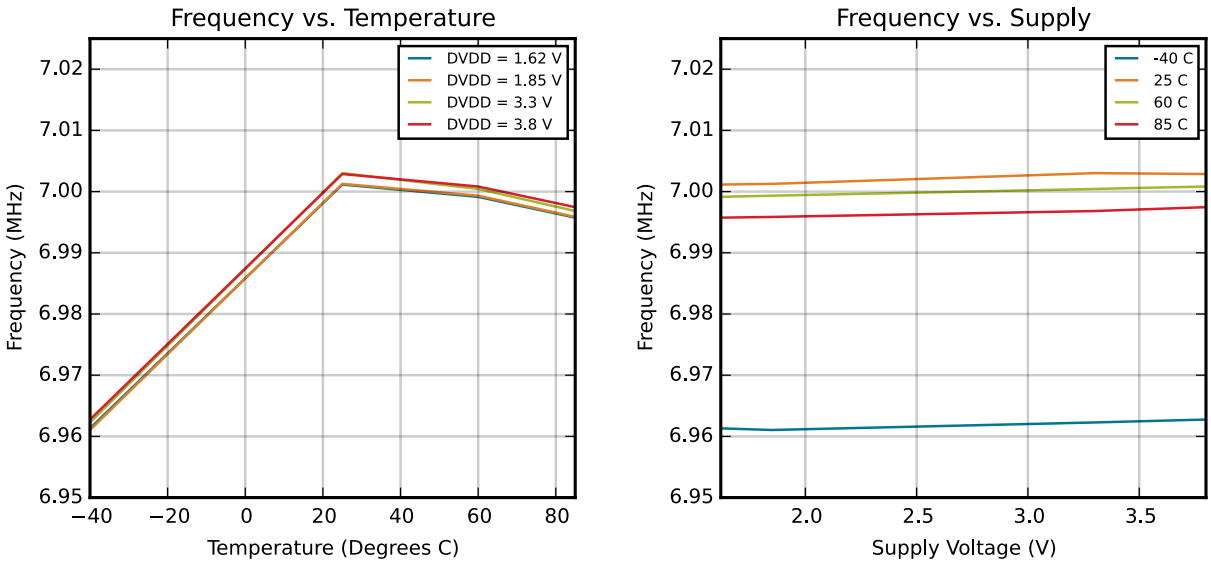


Figure 4.14. HFRCO and AUXHFRCO Typical Performance at 7 MHz

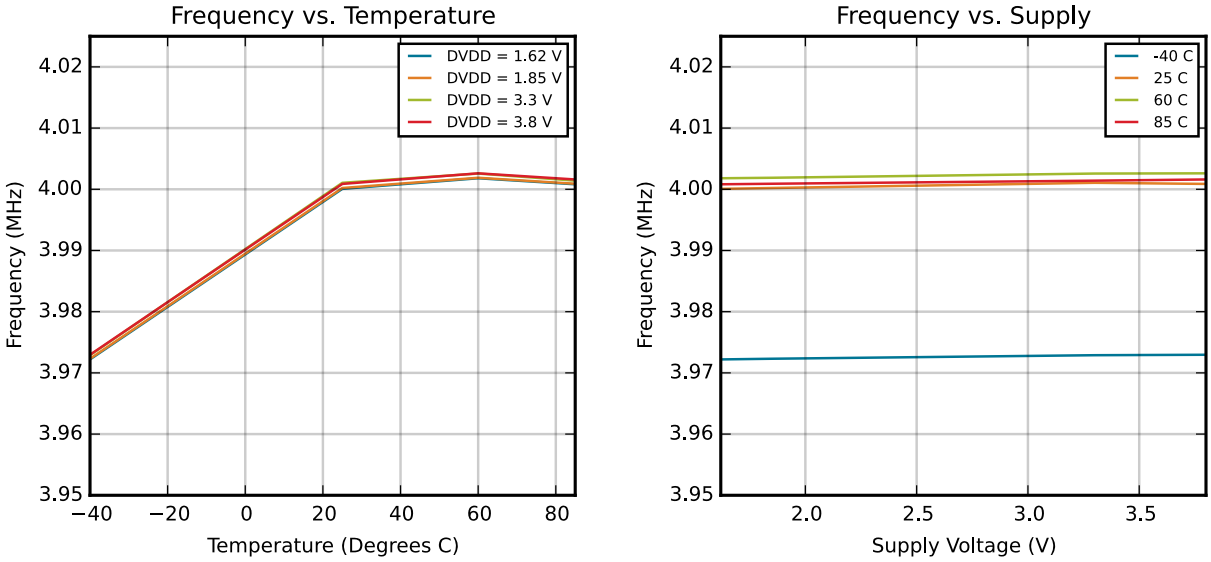


Figure 4.15. HFRCO and AUXHFRCO Typical Performance at 4 MHz

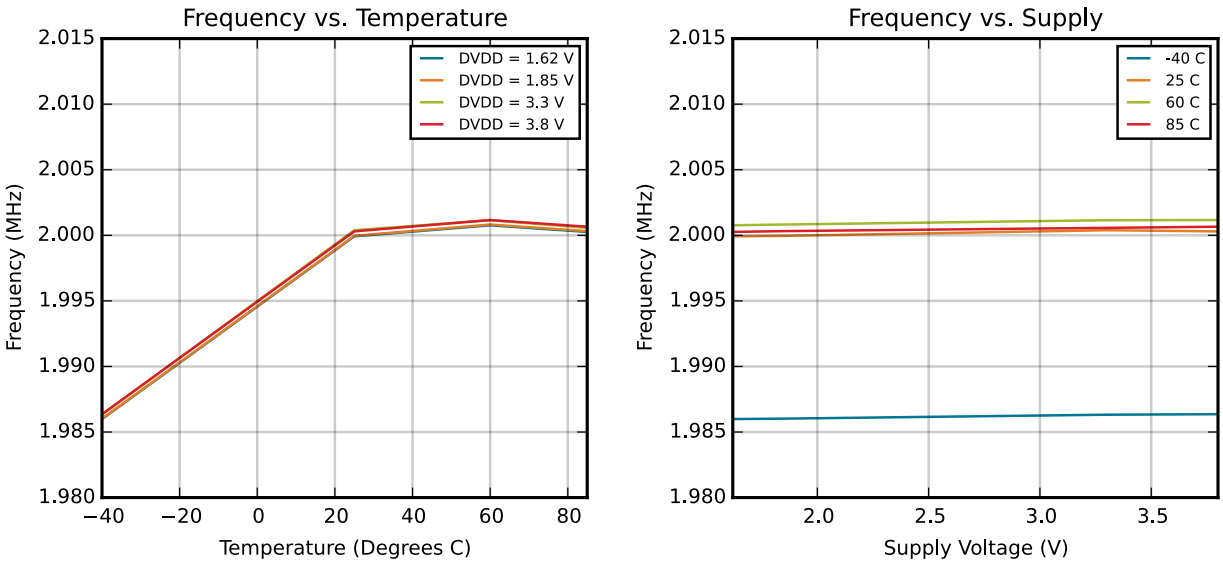


Figure 4.16. HFRCO and AUXHFRCO Typical Performance at 2 MHz

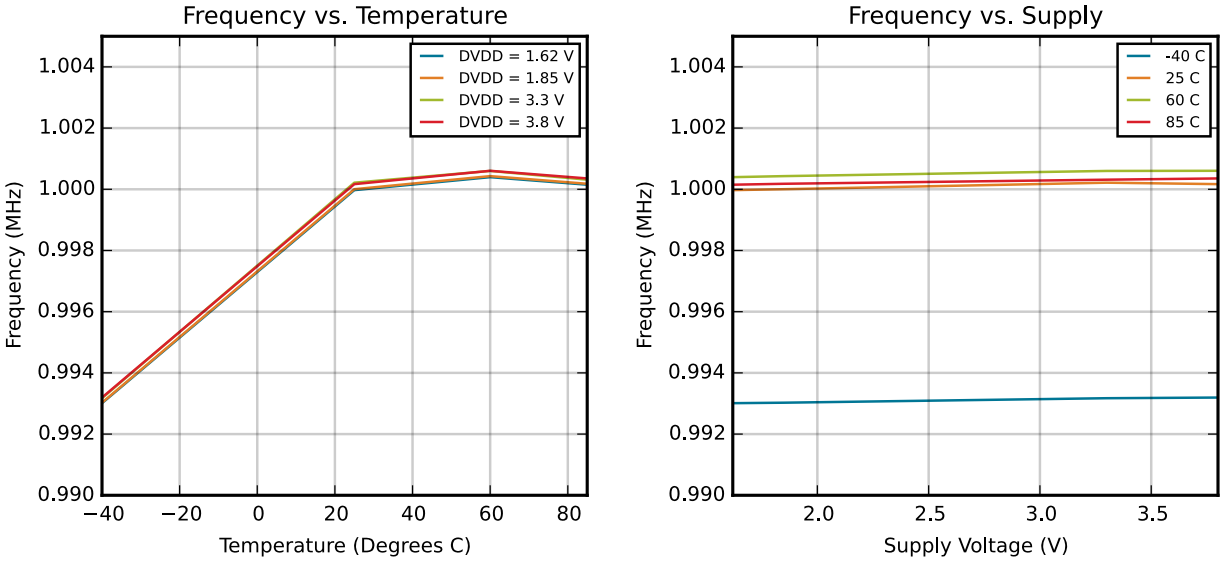


Figure 4.17. HFRCO and AUXHFRCO Typical Performance at 1 MHz

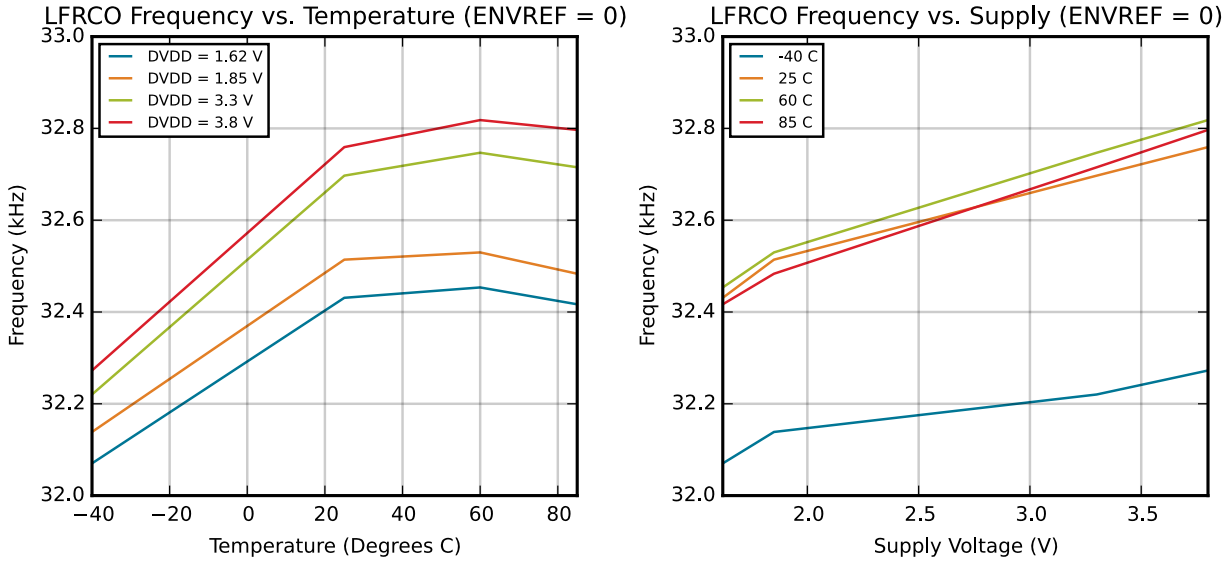


Figure 4.18. LFRCO Typical Performance at 32.768 kHz

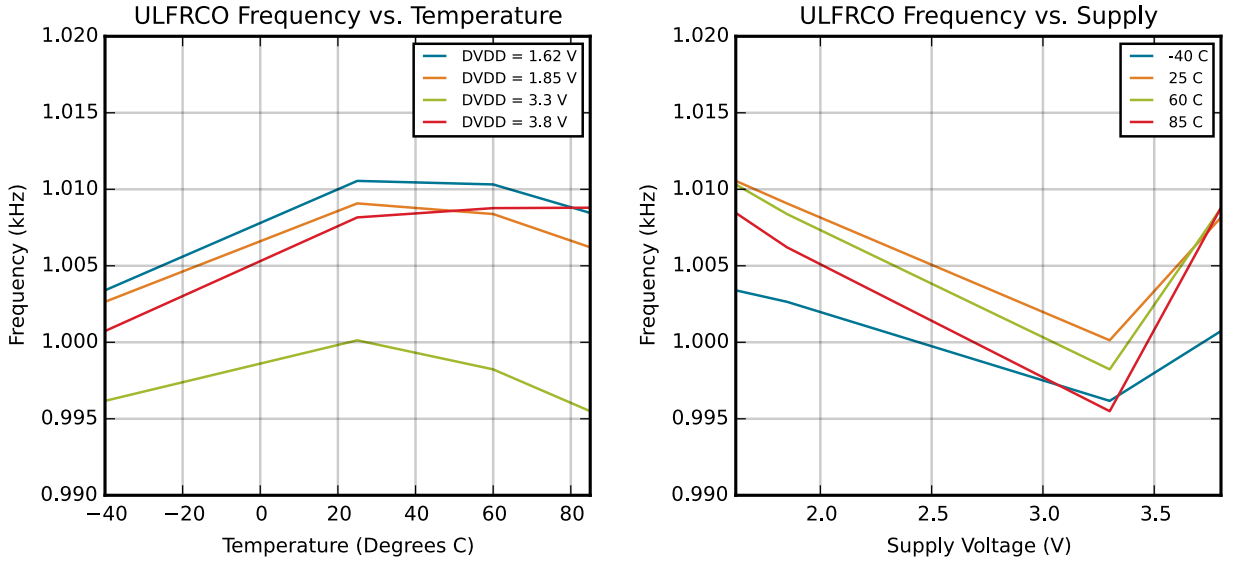


Figure 4.19. ULFRCO Typical Performance at 1 kHz

4.2.4 2.4 GHz Radio

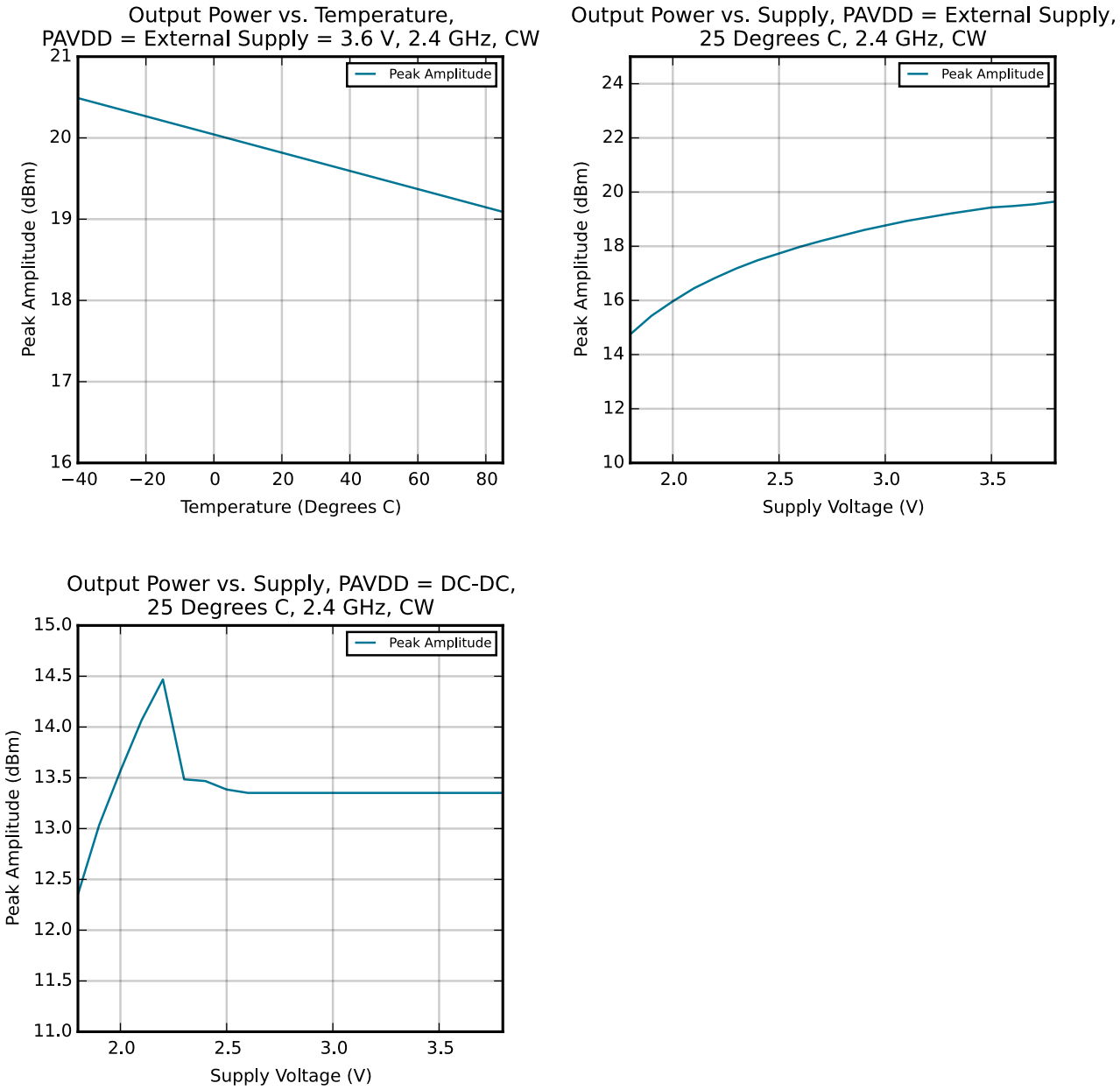


Figure 4.20. 2.4 GHz RF Transmitter Output Power

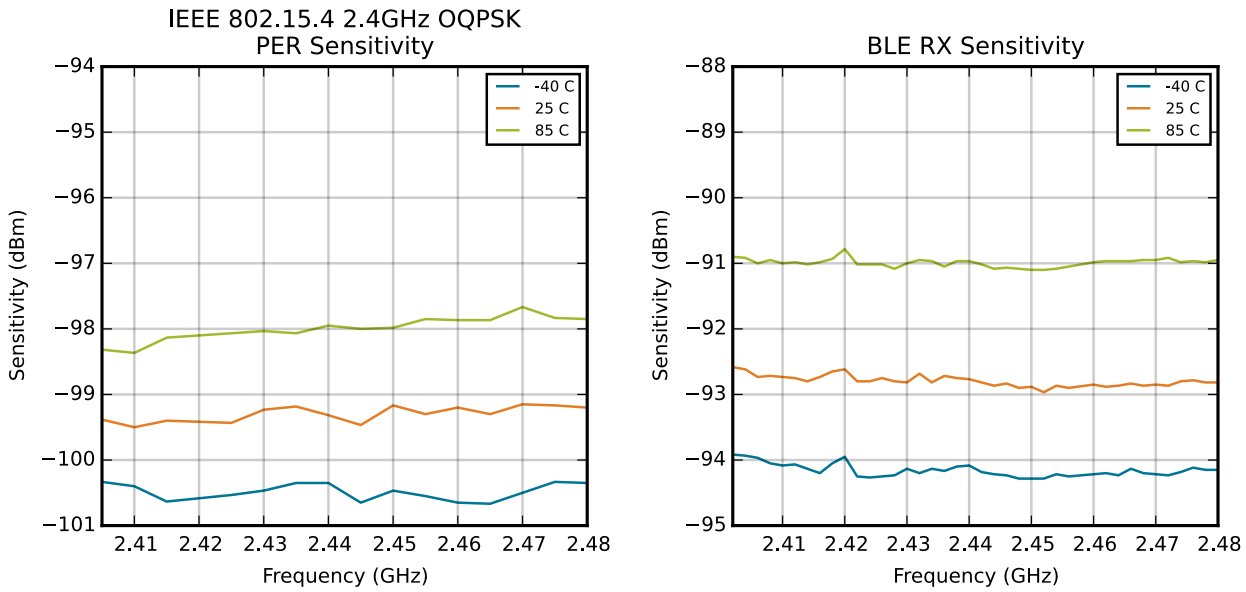


Figure 4.21. 2.4 GHz RF Receiver Sensitivity

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in the following figure.

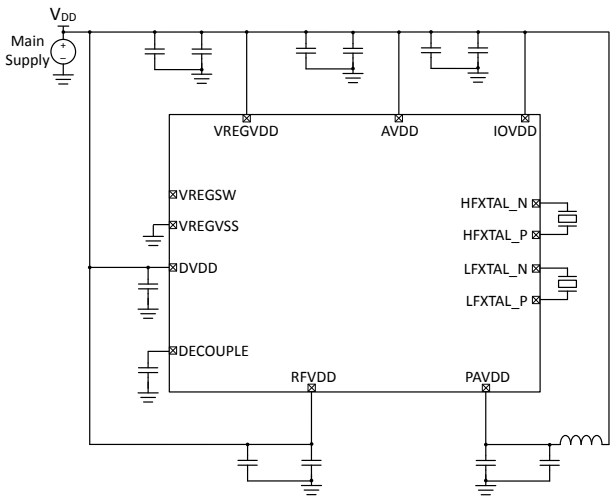


Figure 5.1. EFR32BG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter

Typical power supply circuits using the internal DC-DC converter are shown below. The MCU operates from the DC-DC converter supply. For low RF transmit power applications less than 13dBm, the RF PA may be supplied by the DC-DC converter. For OPNs supporting high power RF transmission, the RF PA must be directly supplied by VDD for RF transmit power greater than 13 dBm.

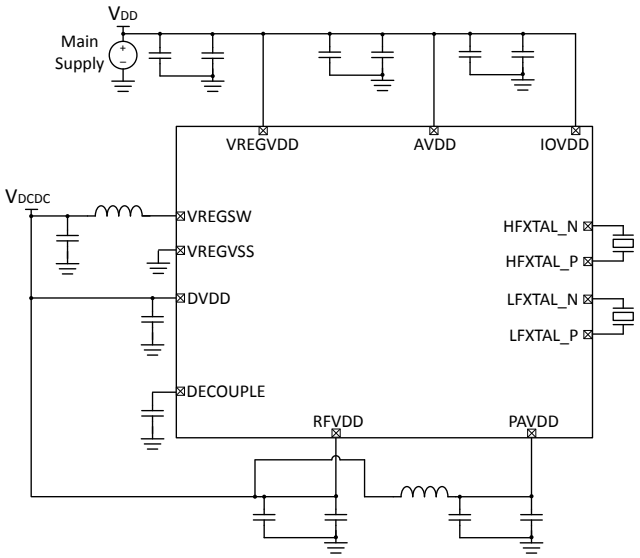


Figure 5.2. EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC)

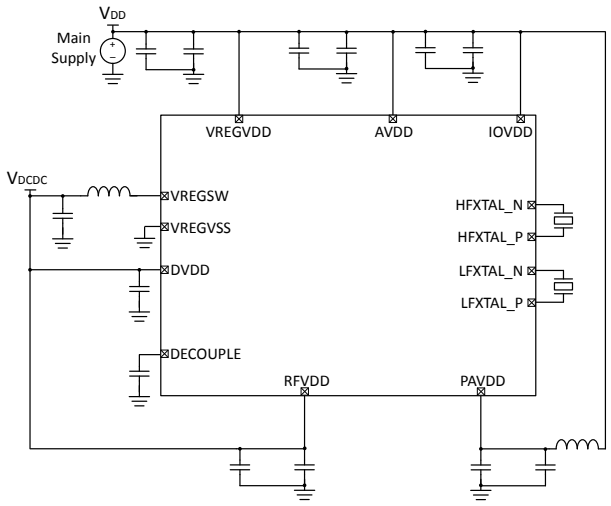


Figure 5.3. EFR32BG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDD)

5.2 RF Matching Networks

Typical RF matching network circuit diagrams are shown in Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 65 for applications in the 2.4GHz band. Application-specific component values can be found in the . For low RF transmit power applications less than 13dBm, the two-element match is recommended. For OPNs supporting high power RF transmission, the four-element match is recommended for high RF transmit power (> 13dBm).

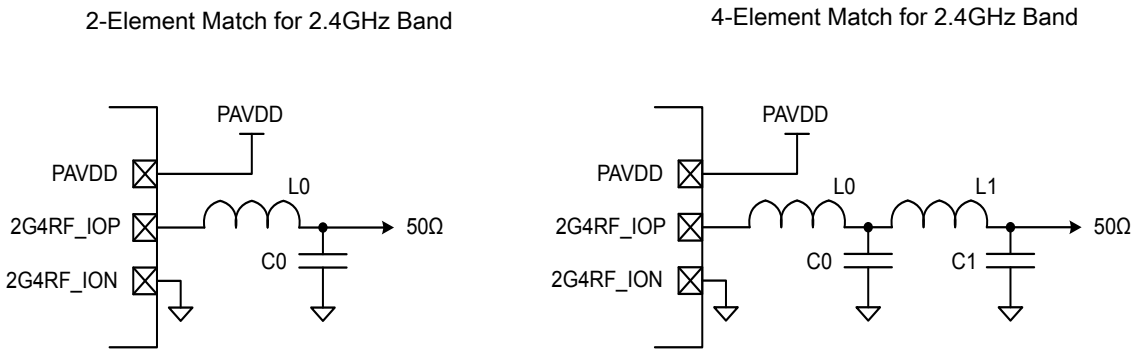


Figure 5.4. Typical 2.4 GHz RF impedance-matching network circuits

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 EFR32BG1 CSP43 2.4 GHz Definition

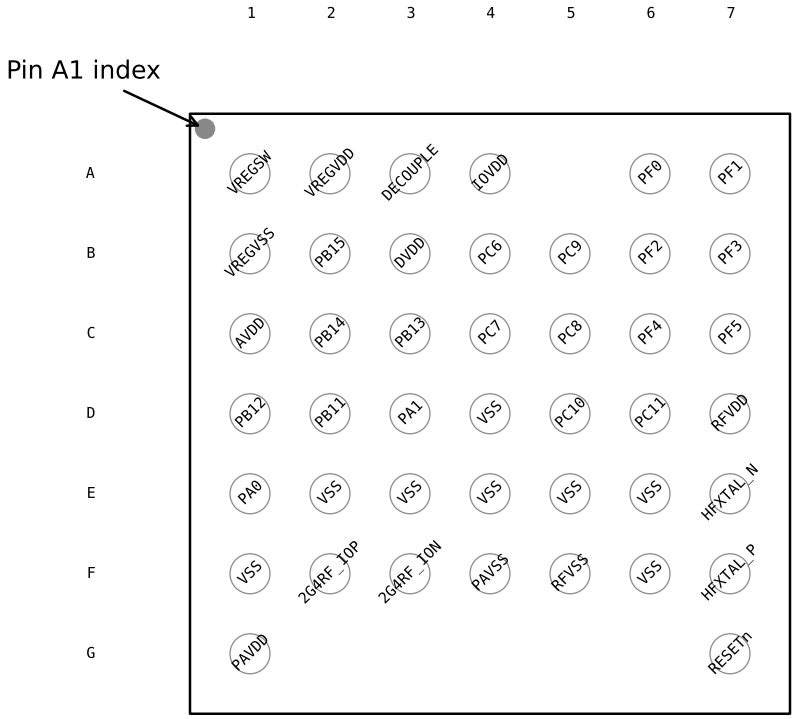


Figure 6.1. EFR32BG1 CSP43 2.4 GHz Pinout

Table 6.1. CSP43 2.4 GHz Device Pinout

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
A1	VREGSW	DCDC regulator switching node				
A2	VREGVDD	Voltage regulator VDD input				
A3	DECOUPLE	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.				
A4	IOVDD	Digital IO power supply.				
A6	PF0	BUSAX BUSBY	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0
A7	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23 MODEM_ANT0 #22 MODEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0
B1	VREGVSS	Voltage regulator VSS				

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
B2	PB15	LFXTAL_P BUSCY BUSDX	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE- TIM0_OUT0 #10 LETIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8 MODEM_ANT0 #7 MODEM_ANT1 #6	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
B3	DVDD	Digital power supply.				
B4	PC6	BUSAX BUSBY	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE- TIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MODEM_DOUT #9 MODEM_ANT0 #8 MODEM_ANT1 #7	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
B5	PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MODEM_DOUT #12 MODEM_ANT0 #11 MODEM_ANT1 #10	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
B6	PF2	BUSAX BUSBY	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24 MODEM_ANT0 #23 MODEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0
B7	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
C1	AVDD	Analog power supply.				
C2	PB14	LFXTAL_N BUSCX BUSDY	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE- TIM0_OUT0 #9 LE- TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7 MODEM_ANT0 #6 MODEM_ANT1 #5	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
C3	PB13	BUSCY BUSDX	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
C4	PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MODEM_DOUT #10 MODEM_ANT0 #9 MODEM_ANT1 #8	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
C5	PC8	BUSAX BUSBY	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MODEM_DOUT #11 MODEM_ANT0 #10 MODEM_ANT1 #9	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
C6	PF4	BUSAX BUSBY	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LETIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26 MODEM_ANT0 #25 MODEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
C7	PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LETIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27 MODEM_ANT0 #26 MODEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
D1	PB12	BUSCX BUSDY	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
D2	PB11	BUSCY BUSDX	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
D3	PA1	ADC0_EXTP BUSCY BUSDX	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
D4	VSS	Ground				
D5	PC10	BUSAX BUSBY	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13 MODEM_ANT0 #12 MODEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12

CSP Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
D6	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE-TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14 MODEM_ANT0 #13 MODEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3
D7	RFVDD	Radio power supply				
E1	PA0	ADC0_EXTN BUSCX BUSDY	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
E2	VSS	Ground				
E3	VSS	Ground				
E4	VSS	Ground				
E5	VSS	Ground				
E6	VSS	Ground				
E7	HFXTAL_N	High Frequency Crystal input pin.				
F1	VSS	Ground				
F2	2G4RF_IOP	2.4 GHz Differential RF input/output, positive path.				
F3	2G4RF_ION	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.				
F4	PAVSS	Power Amplifier (PA) voltage regulator VSS				
F5	RFVSS	Radio Ground				
F6	VSS	Ground				
F7	HFXTAL_P	High Frequency Crystal output pin.				
G1	PAVDD	Power Amplifier (PA) voltage regulator VDD input				
G7	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				

6.1.1 EFR32BG1 CSP43 2.4 GHz GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.2. CSP43 2.4 GHz GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB13, PB12, and PB11 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.3. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	6: PF2							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	6: PF3							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWO	0: PF2 1: PB13 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function is enabled to pin out of reset.
FRC_DCLK	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Frame Controller, Data Sniffer Clock.
FRC_DFRAME		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11		22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	I2C0 Serial Clock Line input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
I2C0_SDA	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.
MODEM_ANT0	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11		21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5	29: PA0 30: PA1	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11		20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5	28: PA0 29: PA1	MODEM antenna control output 1, used for antenna diversity.
MODEM_DCLK	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	MODEM data clock out.
MODEM_DIN	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	MODEM data in.
MODEM_DOUT		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11		22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	30: PA0 31: PA1	MODEM data out.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PCNT0_S0IN	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5	5: PF0 6: PF1 7: PF2							Peripheral Reflex System PRS, channel 3.
PRS_CH6	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15						Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Timer 0 Capture Compare input / output channel 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM0_CC1	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11		22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11		21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5	29: PA0 30: PA1	Timer 0 Compli-mentary Dead Time Insertion channel 0.
TIM0_CDTI1	2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11		20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5	28: PA0 29: PA1	Timer 0 Compli-mentary Dead Time Insertion channel 1.
TIM0_CDTI2	1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 27: PA0	28: PA1	Timer 0 Compli-mentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11		22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11		21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5	29: PA0 30: PA1	Timer 1 Capture Compare input / output channel 3.
US0_CLK		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11		22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	30: PA0 31: PA1	USART0 clock in-put / output.
US0_CS	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11		21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5	29: PA0 30: PA1	USART0 chip se-lect input / output.
US0_CTS	2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11		20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5	28: PA0 29: PA1	USART0 Clear To Send hardware flow control input.
US0_RTS	1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 27: PA0	28: PA1	USART0 Request To Send hardware flow control output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US0_RX	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK		4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11		22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	30: PA0 31: PA1	USART1 clock input / output.
US1_CS	3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11		21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5	29: PA0 30: PA1	USART1 chip select input / output.
US1_CTS	2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11		20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5	28: PA0 29: PA1	USART1 Clear To Send hardware flow control input.
US1_RTS	1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 27: PA0	28: PA1	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1	5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11		24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

6.3 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. A complete description of APORT functionality can be found in the Reference Manual.

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.4. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.5. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.6. ADC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.7. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT1Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	

7. CSP Package Specifications

7.1 CSP Package Dimensions

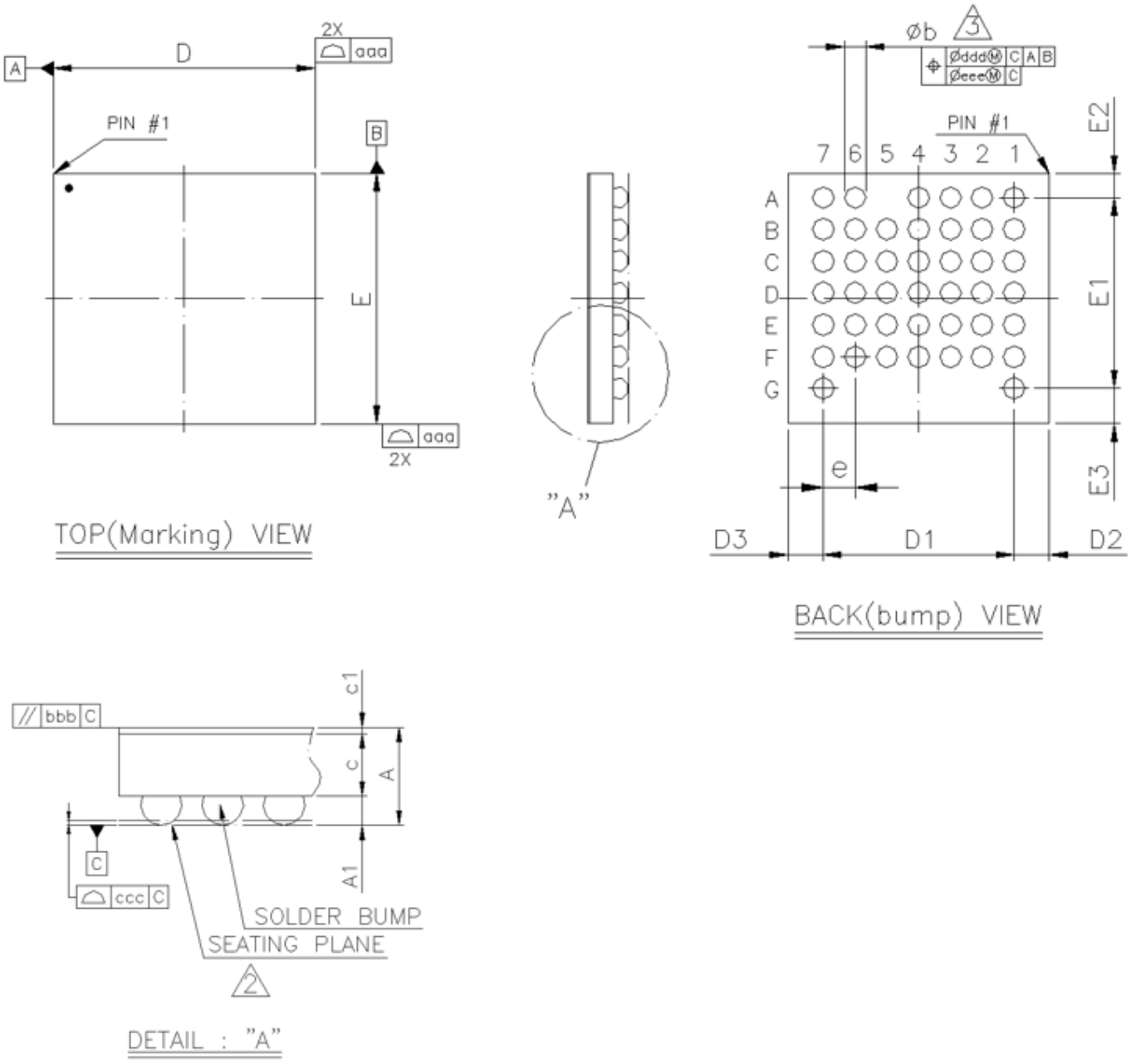


Figure 7.1. CSP Package Drawing

Table 7.1. CSP Package Dimensions

Dimension	Min	Typ	Max
A	0.480	0.510	0.540
A1	0.175	0.190	0.205
c	0.270	0.295	0.320
c1	0.022	0.025	0.028
D	3.260	3.295	3.320
E	3.108	3.143	3.168
b	0.240	0.270	0.300
D1	—	2.400	—
E1	—	2.400	—
D2	—	0.447	—
E2	—	0.302	—
D3	—	0.448	—
E3	—	0.441	—
e	—	0.400	—
aaa	0.10		
bbb	0.10		
ccc	0.03		
ddd	0.15		
eee	0.05		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Minimum bump pitch 0.4mm.
6. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 CSP PCB Land Pattern

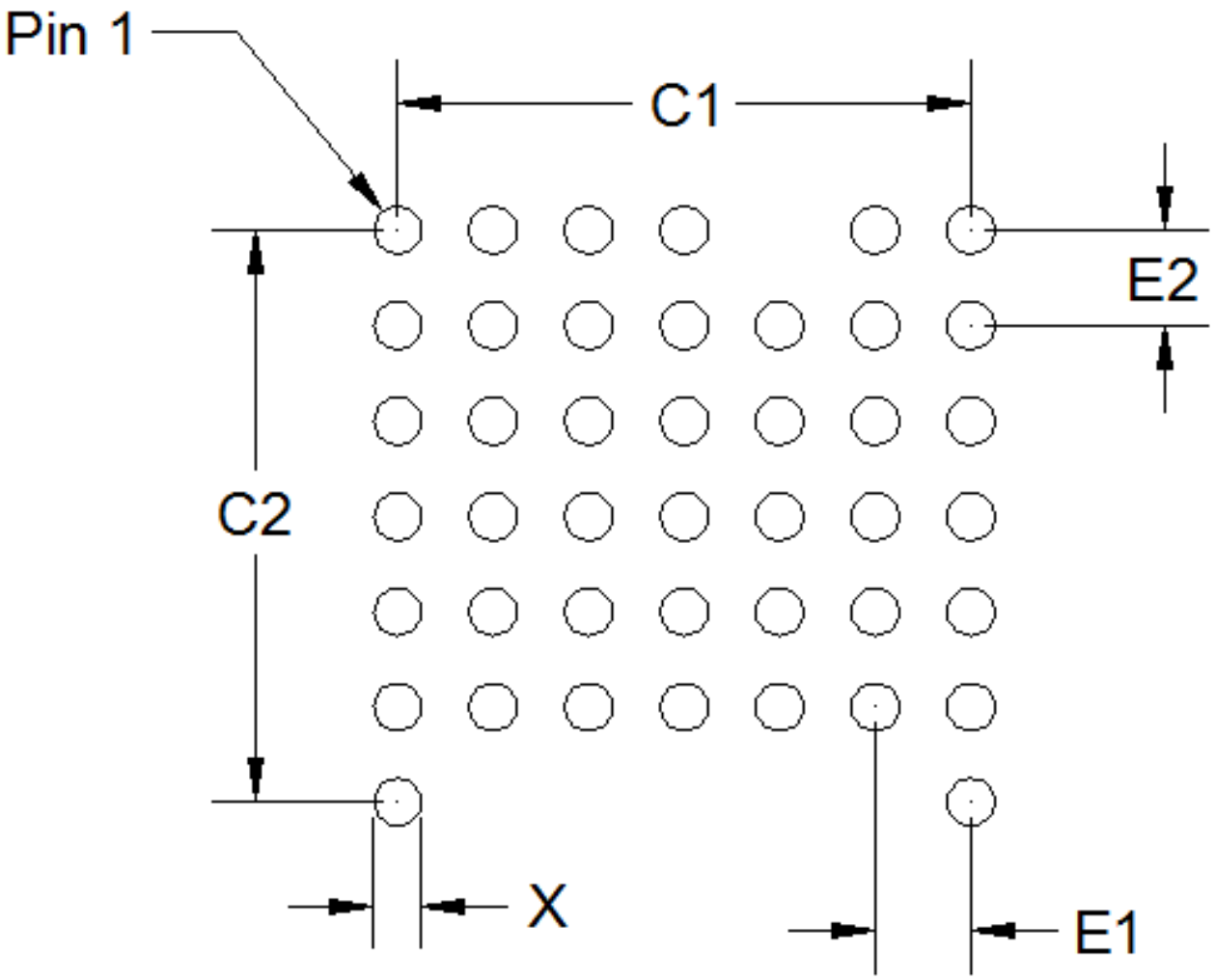


Figure 7.2. CSP PCB Land Pattern Drawing

Table 7.2. CSP PCB Land Pattern Dimensions

Dimension	Typ
X	0.20
C1	2.40
C2	2.40
E1	0.40
E2	0.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.075 mm (3 mils).
7. A stencil of square aperture (0.22 x 0.22 mm) is recommended.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 CSP Package Marking

Figure 7.3. CSP Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (1, 2,...)
  4. Performance Grade (P | B | V)
  5. Feature Code (1 to 7)
  6. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  7. Band (2 = 2.4 GHz)
  8. Flash (G = 256K | F = 128K | E = 64K | D = 32K)
  9. Temperature Grade (G = -40 to 85)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – Bootloader revision number.

8. Revision History

8.1 Revision 1.1

2016-Oct-26

- Ordering Information: Removed Encryption column. All products in family include full encryption capabilites. Previously EFR32BG1V devices listed as "AES only".
- System Overview Sections: Minor wording and typographical error fixes.
- Electrical Characteristics: Minor wording and typographical error fixes.
- "Current Consumption 3.3V with DC-DC" table in Electrical Characteristics: Typical values for EM2 and EM3 current updated with correct values from silicon characterization.
- Pinout tables: APORT channel details removed from "Analog" column. This information is now found in the APORT client map sections.
- Updated APORT client map sections.

8.2 Revision 0.98

2016-July-6

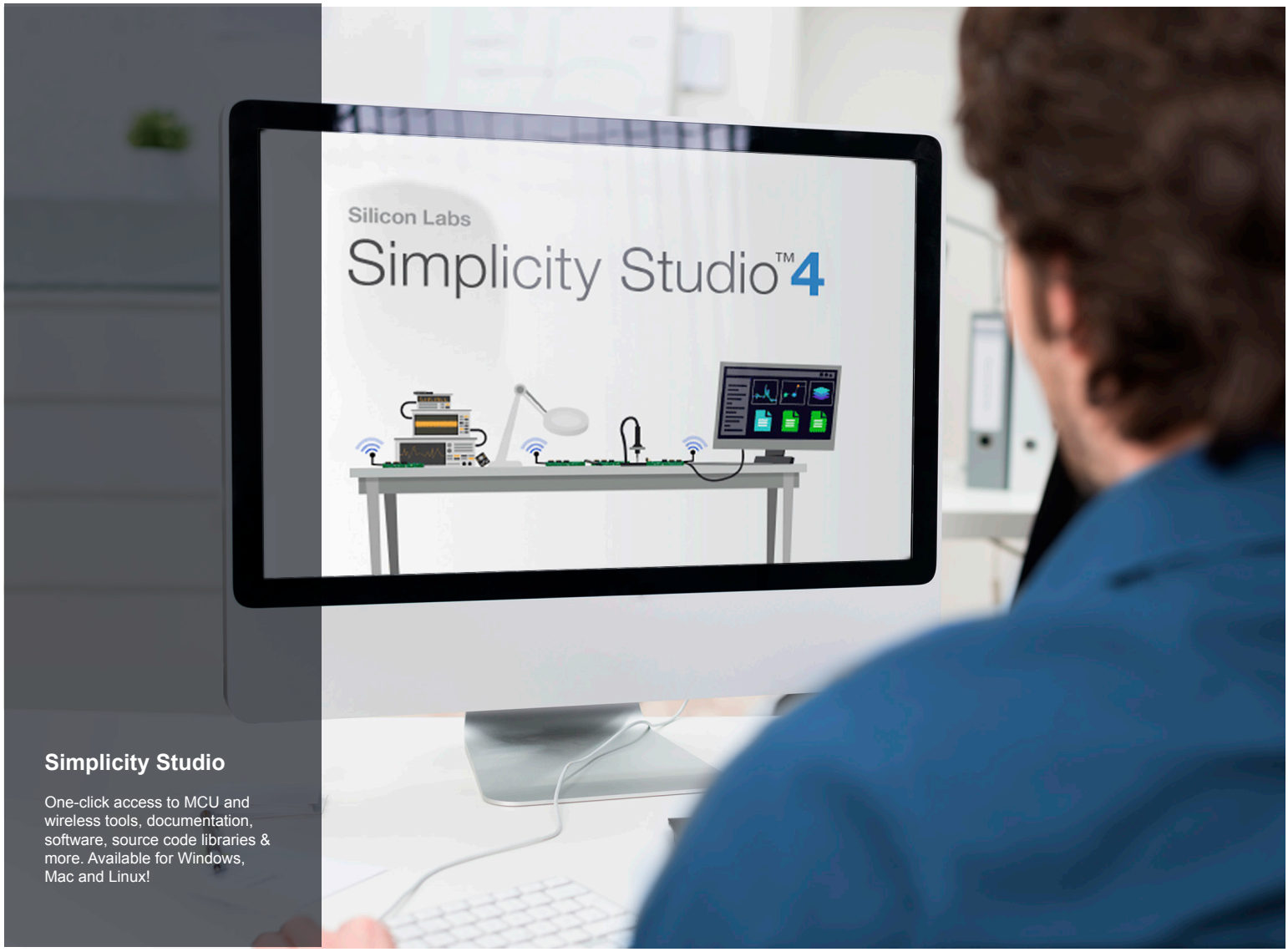
- All OPNs changed to rev C0. Note the following:
  - All OPNs ending in -B0 are Engineering Samples based on an older revision of silicon and are being removed from the OPN table. These older revisions should be used for evaluation only and will not be supported for production.
  - OPNs ending in -C0 are the Current Revision of Silicon and are intended for production.
- Updated OPN table to new format.
- Updated OPN decoder figure to include extended family options.
- Added supported modulation formats and protocols to feature list for P-grade devices.
- Electrical specification tables updated with latest characterization data and production test limits.
- Added graphs in typical performance curves for supply current, oscillator frequency and RF.
- Updated DC-DC graphs in typical performance section.
- Typical connection diagram formatting updated.
- Pinout diagram formatting updated.
- Removed BOOT_TX and BOOT_RX alternate functions from pin function tables.
- Updated package marking diagram with latest inclusive version.

8.3 Revision 0.3

2015-11-2

Initial release of CSP package document.

Table of Contents



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