Wireless Gecko
EFR32BG24 Errata

This document contains information on the EFR32BG24 errata. The latest available revision of this device is revision B.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: March, 2022.

1. Errata Summary

The table below lists all known errata for the EFR32BG24 and all unresolved errata in revision B of the EFR32BG24.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			A	B
CUR_E302	Extra EM1 Current if FPU is Disabled	Yes	X	X
CUR_E303	Active Charge Pump Clock Causes High Current	Yes	X	—
DCDC_E302	DCDC Interrupts Block EM2/3 Entry or Cause Unexpected Wake-up	Yes	X	—
EMU_E304	Higher Than Expected EM2 Current	No	X	—
EUSART_E302	Synchronous EUSART Module Disable Lockup	Yes	X	X
IADC_E306	Changing Gain During a Scan Sequence Causes an Erroneous IADC Result	Yes	X	X
KEYSCAN_E301	Unused Rows Are Not Properly Gated Off	Yes	X	X
RADIO_E305	Channel Clear Detection	No	X	—
RADIO_E307	BLE 2 Mbps and IEEE 802.15.4 Sensitivity Degradation with 38 MHz and 38.4 MHz Crystals	No	X	X
USART_E304	PRS Transmit Unavailable in Synchronous Secondary Mode	No	X	X

2. Current Errata Descriptions

2.1 CUR_E302 – Extra EM1 Current if FPU is Disabled

Description of Errata
When the Floating Point Unit (FPU) is disabled, the on-demand Fast Startup RC Oscillator (FSRCO) remains on after an energy mode transition from EM0 to EM1 is complete. This leads to higher current consumption in EM1.
Affected Conditions / Impacts
The enabled FSRCO increases EM1 current consumption by ~500 µA.
Workaround
Always enable the FPU at the beginning of code execution via the Coprocessor Access Control Register (CPACR) in the System Control Block (SCB) as shown below: `SCB->CPACR |= ((3 << 20) | (3 << 22));`
Resolution
There is currently no resolution for this issue.

2.2 EUSART_E302 — Synchronous EUSART Module Disable Lockup

Description of Errata
The EUSART freezes and does not function if firmware: 1. Initializes the EUSART in synchronous main mode. 2. Disables the EUSART and reconfigures it to either synchronous secondary or asynchronous mode. 3. Re-enables the ESUART. 4. Transfers data. 5. Disables the EUSART. This issue is caused by the failure of a handshake signal that is required by the EUSART disabling logic to fully propagate when leaving synchronous main mode.
Affected Conditions / Impacts
Systems that use the EUSART in synchronous main mode cannot simply switch to another mode as this causes the module to freeze. This ocurs only when firmware attempts to switch from synchronous main mode to another mode. Switching between all other modes is unaffected.
Workaround

Firmware can manually generate additional clock edges after the module is disabled to fully propagate the handshake signal and allow the next disable sequence to happen as usual.
Example code
`//Work-around code//`
`uint32_t i;`
`for (i=0;i<4;i++) {`
`EUSART0->CFG2 |= EUSART_CFG2_CLKPHA;`
`EUSART0->CFG2 &= ~EUSART_CFG2_CLKPHA;`
`}`
`//Work-around code - END//`

Resolution
There is currently no resolution for this issue.

2.3 IADC_E306 – Changing Gain During a Scan Sequence Causes an Erroneous IADC Result

Description of Errata
Differences in the ANALOGGAIN setting within multiple IADC_CFGx groups during a scan sequence introduces a transient condition that may result in an inaccurate IADC conversion.
Affected Conditions / Impacts
The result of the IADC scan measurement may not match the expected result for the voltage present on the pin during the conversion.
Workaround
Both 1 and 2 shown below must be implemented. 1. If there is a difference in the ANALOGGAIN setting between IADC_CFGx groups during a scan sequence, the IADC_SCHEDx clock prescaler must also change to an appropriate setting. This forces a warmup state (5µs delay) in between ANALOGGAIN changes. Please note that the same IADC_SCHEDx clock prescaler value may be an appropriate setting for both ANALOGGAIN settings, but in order to force the warmup delay, the IADC_SCHEDx must have different values. 2. The first and last entry of a scan group should use IADC_CFG0, which is the default configuration of the IADC at the start and end of a scan conversion sequence. If CONFIG1 is used at the start and end of the scan group, erronous IADC results may occur.
Resolution
There is currently no resolution for this issue.

2.4 KEYSCAN_E301 – Unused Rows Are Not Properly Gated Off

Description of Errata
Unused KEYSCAN row inputs cause the KEY bit in the KEYSCAN_IF register to be set at all times indicating a key was pressed. This prevents the interrupt flag from clearing and stops the scan procedure.
Affected Conditions / Impacts
The KEY bit in the KEYSCAN_IF register is always set when rows are left unused.
Workaround

Configure the GPIO_KEYSCAN_ROWSENSEnROUTE registers for any unused row inputs to the same GPIO port and pin associated with any of the row inputs that are used. For example, if rows 0, 1, and 2 are used and routed to PA05, PA06, and PA07 respectively, and rows 3, 4, and 5 are unused, the configuration could be:
`// Routing GPIO pins PA05, PA06 and PA07 to rows 0, 1 and 2`
`GPIO->DBUSKEYPAD_ROWSENSE0ROUTE = 0 << _GPIO_DBUSKEYPAD_ROWSENSE0ROUTE_PORT_SHIFT |`
`5 << _GPIO_DBUSKEYPAD_ROWSENSE0ROUTE_PIN_SHIFT;`
`GPIO->DBUSKEYPAD_ROWSENSE1ROUTE = 0 << _GPIO_DBUSKEYPAD_ROWSENSE1ROUTE_PORT_SHIFT|`
`6 << _GPIO_DBUSKEYPAD_ROWSENSE1ROUTE_PIN_SHIFT;`
`GPIO->DBUSKEYPAD_ROWSENSE2ROUTE = 0 << _GPIO_DBUSKEYPAD_ROWSENSE2ROUTE_PORT_SHIFT|`
`7 << _GPIO_DBUSKEYPAD_ROWSENSE2ROUTE_PIN_SHIFT;`
 	
`// Workaround - Connect unused rows 3, 4, and 5 to row 2 (PA07), a single used row`
`GPIO->KEYPADROUTE.ROWSENSE3ROUTE = 0 << _GPIO_KEYSCAN_ROWSENSE3ROUTE_PORT_SHIFT |`
`7 << _GPIO_KEYSCAN_ROWSENSE3ROUTE_PIN_SHIFT;`
`GPIO->KEYPADROUTE.ROWSENSE4ROUTE = 0 << _GPIO_KEYSCAN_ROWSENSE4ROUTE_PORT_SHIFT |`
`7 << _GPIO_KEYSCAN_ROWSENSE4ROUTE_PIN_SHIFT;`
`GPIO->KEYPADROUTE.ROWSENSE5ROUTE = 0 << _GPIO_KEYSCAN_ROWSENSE5ROUTE_PORT_SHIFT |`
`7 << _GPIO_KEYSCAN_ROWSENSE5ROUTE_PIN_SHIFT;`
 	
Note that KEYSCAN_STATUS.ROW will report the same values for used and unused rows that route to the same GPIO. In the scenario above, KEYSCAN_STATUS.ROW bits 2, 3, 4, and 5 will show the same values. The unused row bits in the KEYSCAN_STATUS field should be masked so that unused row bits are set to 1, indicating a key is not pressed.

Resolution
There is currently no resolution for this issue.

2.5 RADIO_E307 – BLE 2 Mbps and IEEE 802.15.4 Sensitivity Degradation with 38 MHz and 38.4 MHz Crystals

Description of Errata
Sensitivity degradation of approximately 8 dB using the BLE 2 Mbps or 802.15.4 PHYs when using crystals below 39 MHz.
Affected Conditions / Impacts
The BLE 2 Mbps PHY and 802.15.4 PHY will show a degradation of approximately 8 dB at higher frequencies when using crystals below 39 MHz. For the 38 MHz crystal, the degradation will be seen at 2432 MHz and above. For the 38.4 MHz crystal, the degradation will be seen at 2458 MHz and above. This problem does not exist with 39 MHz and above crystals. The BLE 1 Mbps and LR PHYs are unaffected.
Workaround
There is currently no workaround for either a 38 MHz or 38.4 MHz crystal. Use of a 39 MHz or 40 MHz crystal avoids the sensitivity degradation.
Resolution
There is currently no resolution for this issue.

2.6 USART_E304 — PRS Transmit Unavailable in Synchronous Secondary Mode

Description of Errata
When the USART is configured for synchronous secondary operation, the transmit output (MISO) is not driven if the signal is routed to a pin using the PRS producer (e.g., SOURCESEL = 0x20 and SIGSEL = 0x4 for USART0).
Affected Conditions / Impacts
Systems cannot operate the USART in synchronous secondary mode if the PRS is used to route the transmit output to the RX (MISO) pin. Operation is not affected in main mode when the transmit output is routed to the TX (MOSI) pin using the PRS producer nor is operation affected in any mode when the GPIO_USARTn_RXROUTE and GPIO_USARTn_TXROUTE registers are used.
Workaround
There is currently no workaround for this issue.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EFR32BG24 devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 CUR_E303 – Active Charge Pump Clock Causes High Current

Description of Errata
When the ACMP0, ACMP1, or IADC0 peripherals are active, the clock to the internal analog mux charge pump may also be activated, resulting in extra supply current.
Affected Conditions / Impacts
• ACMP0 and ACMP1: The charge pump clock is activated whenever either module is enabled via the ACMPn_EN_EN bit or when enabled by the LESENSE state machine. • IADC0: The charge pump clock is activated when any portion of the IADC analog circuitry is on. When IADC_CTRL_WARMUP-MODE = KEEPINSTANDBY or KEEPWARM, the clock is activated as long as the IADC is enabled via the IADC_EN_EN bit. When IADC_CTRL_WARMUPMODE = NORMAL, the clock is activated only during warmup and conversion and will be shut down be-tween conversions. • The extra current is from a shared block and increases supply current by an approximate total of 25 µA when any of the above conditions are true.
Workaround
No workaround exists to entirely eliminate the extra current. The impact of the current can be reduced by duty-cycling the peripheral. The average system supply current increase depends on the total percentage of time the peripheral(s) is/are active. For example, if only ACMP0 is used and enabled for 10% of the time, the average supply current increase is about 2.5 µA.
Resolution
This issue is resolved in revision B devices.

3.2 DCDC_E302 – DCDC Interrupts Block EM2/3 Entry or Cause Unexpected Wake-up

Description of Errata
Regardless of DCDC_IEN setting, if the DCDC interrupt is enabled in the NVIC, any of the four DCDC interrupt sources (DCDC_IF_WARM, DCDC_IF_RUNNING, DCDC_IF_TMAX, and DCDC_IF_BYPSW) can wake the device from EM2/3 or prevent it from entering EM2/3.
Affected Conditions / Impacts
The errata is limited to the DCDC_IF_WARM, DCDC_IF_RUNNING, DCDC_IF_TMAX and DCDC_IF_BYPSW requests, which also function as wake-up sources from EM2/3. When the NVIC DCDC interrupt source is enabled: • If IEN for one of these interrupt requests is set to 1 and that condition occurs, then an interrupt *will* occur and the CPU will branch to the DCDC IRQ handler. • If IEN for one of these interrupt sources is cleared to 0 and that condition occurs, then an interrupt *will not* occur. • If any of these four interrupt conditions occurs, regardless of the setting of their corresponding DCDC_IEN bits, the device *will* wake from EM2/3 and/or be prevented from entering EM2/3. If the corresponding IEN was not set, an interrupt *will not* occur even though the EM2/3 wakeup event has occurred.
Workaround
To prevent unwanted wake-up from or blocked entry into EM2/3, disable the DCDC interrupt using `NVIC_DisableIRQ(DCDC_IRQn)` before entering EM2/3 and re-enable the DCDC interrupt using `NVIC_EnableIRQ(DCDC_IRQn)` after EM2/3 wake-up.
Resolution
This issue is resolved in revision B devices.

3.3 EMU_E304 – Higher Than Expected EM2 Current

Description of Errata
Current consumption in EM2 is higher than the datasheet specification.
Affected Conditions / Impacts
Systems operating in EM2 have higher than expected current consumption, regardless of whether the DCDC is enabled.
Workaround
There is currenty no workaround for this issue.
Resolution
This issue is resolved in revision B devices.

3.4 RADIO_E305 – Channel Clear Detection

Description of Errata
The Listen Before Talk (LBT) and Carrier Sense Multiple Access-Collision Avoidance (CSMA-CA) algorithms always indicate that the channel is clear, even when this is not the case.
Affected Conditions / Impacts
The LBT and CSMA-CA algorithms cannot be used.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B devices.

4. Revision History

Revision 0.4

March, 2022

- Added CUR_E303.
- Added IADC_E306.
- Added KEYSCAN_E301.
- Added RADIO_E307.

Revision 0.3

January, 2022

- Updated for device revision B.
- Resolved and moved DCDC_E302, EMU_E304 and RADIO_E305 to Resolved Errata.
- Added USART_E304.
- Replaced select terms with inclusive lexicon.

Revision 0.2

August, 2021

- Added CUR_E302 and DCDC_E302.

Revision 0.1

June, 2021

- Initial release

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