



# Wireless Gecko EFR32MG27 Errata

---



This document contains information on the EFR32MG27 errata. The latest available revision of this device is revision B. Errata that have been resolved remain documented and can be referenced for previous revisions of this device. The device data sheet explains how to identify the chip revision, either from the package marking or electronically. Errata effective date: August, 2022.

## 1. Errata Summary

The table below lists all known errata for the EFR32MG27 and all unresolved errata of the EFR32MG27.

**Table 1.1. Errata Overview**

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			A	B
EMU_E306	<a href="#">IOVDD Brown-Out Misdetection During Supply Ramp</a>	Yes	X	X
IADC_E306	<a href="#">Changing Gain During a Scan Sequence Causes an Erroneous IADC Result</a>	Yes	X	X
USART_E304	<a href="#">PRS Transmit Unavailable in Synchronous Secondary Mode</a>	No	X	X

## 2. Current Errata Descriptions

### 2.1 EMU\_E306 – IOVDD Brown-Out Misdetection During Supply Ramp

<b>Description of Errata</b>
The IOVDD brown-out detector incorrectly reports a valid operating level when the IOVDD supply begins ramping after DVDD has reached the minimum operating level and the device has been released from reset.
<b>Affected Conditions / Impacts</b>
Because the IOVDD supply is fully decoupled from the DVDD supply, it is permissible for the DVDD supply to lead the IOVDD supply and thus allow the CPU to exit reset and begin executing code before IOVDD has reached a suitable minimum operating voltage for external logic.  In such a configuration, the IOVDD brown-out detector cannot be immediately relied upon to detect a valid operating level because it will inadvertently show that IOVDD is valid over a nominal range of 0.5 V to 0.7 V.  The duration of this misdetection and the specific voltage range over which it occurs vary depending on the ramp rate of IOVDD. Variation is also observed from device to device and over temperature. For slower ramps, the duration is extended and the range adheres more closely to 0.5 V to 0.7 V. For faster ramps, the duration is reduced but the range over which the misdetection occurs can shift to higher voltages. The brown-out detector will settle and report correctly within 1 ms of IOVDD reaching its steady-state level.
<b>Workaround</b>
For a system that might be subject to this condition, select one of the following two workarounds: <ol style="list-style-type: none"> <li>1. Use a power supply configuration in which IOVDD is tied to or ramps concurrently with DVDD.</li> <li>2. Characterize the system's IOVDD ramp time and implement a software delay with some headroom (e.g. via Sleptimer and with the underlying hardware timer clocked from the LFRCO) that must first elapse to account for the misdetection period and before proceeding with the initialization of GPIO pins.</li> </ol> <p><b>Note:</b> The IADC cannot be used to monitor the IOVDD ramp because its supply input multiplexer will not be powered until IOVDD reaches a valid operating level.</p>
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.2 IADC\_E306 – Changing Gain During a Scan Sequence Causes an Erroneous IADC Result

<b>Description of Errata</b>
Differences in the ANALOGGAIN setting within multiple IADC_CFGx groups during a scan sequence introduces a transient condition that may result in an inaccurate IADC conversion.
<b>Affected Conditions / Impacts</b>
The result of the IADC scan measurement may not match the expected result for the voltage present on the pin during the conversion.
<b>Workaround</b>
Both 1 and 2 shown below must be implemented. <ol style="list-style-type: none"> <li>1. If there is a difference in the ANALOGGAIN setting between IADC_CFGx groups during a scan sequence, the IADC_SCHEx clock prescaler must also change to an appropriate setting. This forces a warmup state (5 <math>\mu</math>s delay) in between ANALOGGAIN changes. Note that the same IADC_SCHEx clock prescaler value may be an appropriate setting for both ANALOGGAIN settings, but to force the warmup delay, the IADC_SCHEx must have different values.</li> <li>2. The first and last entry of a scan group should use IADC_CFG0, which is the default configuration of the IADC at the start and end of a scan conversion sequence. If CONFIG1 is used at the start and end of the scan group, erroneous IADC results may occur.</li> </ol>
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.3 USART\_E304 — PRS Transmit Unavailable in Synchronous Secondary Mode

<b>Description of Errata</b>
When the USART is configured for synchronous secondary operation, the transmit output (MISO) is not driven if the signal is routed to a pin using the PRS producer (e.g., SOURCESEL = 0x20 and SIGSEL = 0x4 for USART0).
<b>Affected Conditions / Impacts</b>
Systems cannot operate the USART in synchronous secondary mode if the PRS is used to route the transmit output to the RX (MISO) pin. Operation is not affected in main mode when the transmit output is routed to the TX (MOSI) pin using the PRS producer nor is operation affected in any mode when the GPIO_USARTn_RXROUTE and GPIO_USARTn_TXROUTE registers are used.
<b>Workaround</b>
There is currently no workaround for this issue.
<b>Resolution</b>
There is currently no resolution for this issue.

### 3. Revision History

#### Revision 0.2

August, 2022

- Updated for device revision B.

#### Revision 0.1

May, 2022

- Initial release.

# Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!



**IoT Portfolio**  
[www.silabs.com/IoT](http://www.silabs.com/IoT)



**SW/HW**  
[www.silabs.com/simplicity](http://www.silabs.com/simplicity)



**Quality**  
[www.silabs.com/quality](http://www.silabs.com/quality)



**Support & Community**  
[www.silabs.com/community](http://www.silabs.com/community)

## Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

**Note: This content may contain offensive terminology that is now obsolete. Silicon Labs is replacing these terms with inclusive language wherever possible. For more information, visit [www.silabs.com/about-us/inclusive-lexicon-project](http://www.silabs.com/about-us/inclusive-lexicon-project)**

## Trademark Information

Silicon Laboratories Inc.<sup>®</sup>, Silicon Laboratories<sup>®</sup>, Silicon Labs<sup>®</sup>, SiLabs<sup>®</sup> and the Silicon Labs logo<sup>®</sup>, Bluegiga<sup>®</sup>, Bluegiga Logo<sup>®</sup>, EFM<sup>®</sup>, EFM32<sup>®</sup>, EFR, Ember<sup>®</sup>, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Redpine Signals<sup>®</sup>, WiSeConnect, n-Link, ThreadArch<sup>®</sup>, EZLink<sup>®</sup>, EZRadio<sup>®</sup>, EZRadioPRO<sup>®</sup>, Gecko<sup>®</sup>, Gecko OS, Gecko OS Studio, Precision32<sup>®</sup>, Simplicity Studio<sup>®</sup>, Telegesis, the Telegesis Logo<sup>®</sup>, USBXpress<sup>®</sup>, Zentri, the Zentri logo and Zentri DMS, Z-Wave<sup>®</sup>, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

[www.silabs.com](http://www.silabs.com)