



# Mighty Gecko Lighting Module MGM210L Errata

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This document contains information on the MGM210L errata. The latest available revision of this device is revision 2.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

Errata effective date: September, 2019.

## 1. Errata Summary

The table below lists all known errata for the MGM210L and all unresolved errata in revision 2 of the MGM210L.

**Table 1.1. Errata Overview**

Designator	Title/Problem	Workaround Exists	Exists on Revision:
			2
GPIO_E302	<a href="#">Increased Leakage Current When EM4WU Pins Are Enabled and the Pin State Is High</a>	Yes	X
HFXO_E301	<a href="#">HFXO DISONDEMAND and FORCEEN Can Cause Device to Hang</a>	Yes	X
IADC_E304	<a href="#">Possible Data Loss in EM2/EM3</a>	Yes	X
RADIO_E301	<a href="#">Improper TX and RX Operation at High Temperature</a>	Yes	X
TIMER_E301	<a href="#">Continuous Overflow and Underflow Interrupts in Quadrature Counting Mode</a>	Yes	X

## 2. Current Errata Descriptions

### 2.1 GPIO\_E302 – Increased Leakage Current When EM4WU Pins Are Enabled and the Pin State Is High

<b>Description of Errata</b>
When any of the EM4WU pins are used with the input path enabled and the pin state is high, an extra leakage current of approximately 15 $\mu$ A per pin will be observed in EM0, EM1, EM2, and EM3.
<b>Affected Conditions / Impacts</b>
EM0, EM1, EM2, and EM3 current will be higher by approximately 15 $\mu$ A per pin when any of the EM4WU pins are used with the input path enabled and the pin state is high.
<b>Workaround</b>
There are two workarounds for this issue: <ol style="list-style-type: none"> <li>1. If the input path on the pad is not required, disable the input path on that pad by setting the DINDIS or DINDISALT bits in the GPIO_PORTx_CTRL register. Thus, an EM4WU pin can still be used to drive an output without incurring the extra current leakage when the pin is configured as an output and DINDIS or DINDISALT is set.</li> <li>2. If an input path is required (i.e. MODEN is any value other than DISABLED and DINDIS = 0 or DINDISALT = 0), assign it to a pin which does not have EM4 wakeup capability.</li> </ol> <p>Refer to the device data sheet to determine which pins have or do not have EM4 wake-up functionality.</p>
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.2 HFXO\_E301 — HFXO DISONDEMAND and FORCEEN Can Cause Device to Hang

<b>Description of Errata</b>
When DISONDEMAND and FORCEEN in the HFXO_CTRL register are both 1, the HFXO causes a handshake between the EMU and the CMU to hang, which may prevent a system reset from being asserted.
<b>Affected Conditions / Impacts</b>
The device will hang waiting for the EMU/CMU handshake to complete, requiring a pin reset to recover.
<b>Workaround</b>
Do not set DISONDEMAND = 1 in HFXO_CTRL while the HFXO is enabled.
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.3 IADC\_E304 – Possible Data Loss in EM2/EM3

<b>Description of Errata</b>
When the IADC wakes from EM2 or EM3 and generates conversion results that the LDMA transfers to RAM, it is possible under very rare circumstances to lose data when the ratio of the bus clock (HCLK) is slow compared to the prescaled IADC clock (ADC_CLK).
<b>Affected Conditions / Impacts</b>
Data from IADC conversions in these cases can potentially be lost due to FIFO overflow.
<b>Workaround</b>
To prevent data loss when the IADC awakens from EM2 or EM3 and performs conversions that are serviced by the LDMA before re-entering the low-energy state, make sure that: <ul style="list-style-type: none"><li>• the rate at which the IADC takes samples in EM2 or EM3 is less than or equal to 125 kHz (samples are taken no faster than every 8 <math>\mu</math>s), and</li><li>• the frequency of the HCLK (bus clock) is at least four times the frequency of the IADCCLK.</li></ul>
<b>Resolution</b>
There is currently no resolution for this issue.

### 2.4 RADIO\_E301 – Improper TX and RX Operation at High Temperature

<b>Description of Errata</b>
Some radio transceivers may fail to lock to the correct RF frequency at high operating temperatures when using Gecko SDK prior to Gecko SDK v2.5.4.
<b>Affected Conditions / Impacts</b>
Devices using Gecko SDK prior to v2.5.4 at high operating temperatures may be unable to lock to the desired RF frequency. This may cause errors in the TX/RX frequency or an inability to transmit or receive data.
<b>Workaround</b>
Customers should use firmware provided in Gecko SDK v2.5.4 or later for proper TX/RX operation.
<b>Resolution</b>
There is currently no resolution for this issue.

## 2.5 TIMER\_E301 — Continuous Overflow and Underflow Interrupts in Quadrature Counting Mode

<b>Description of Errata</b>
<p>When the TIMER is configured to operate in quadrature decoder mode with the overflow interrupt enabled and the counter value (TIMER_CNT) reaches the top value (TIMER_TOP), the overflow interrupt is requested continuously even if the interrupt flag (TIMER_IF_OF) is cleared. Similarly, if the underflow interrupt is enabled and the counter value reaches zero, the underflow interrupt is requested continuously even if the interrupt flag (TIMER_IF_UF) is cleared. Only after the counter value has incremented or decremented so that the overflow or underflow condition no longer applies can the interrupt be cleared.</p>
<b>Affected Conditions / Impacts</b>
<p>Because the counter is clocked by its CC0 and CC1 inputs in quadrature decoder mode and not the prescaled HPPERCLK, overflow and underflow events remain latched as long TIMER_CNT remains at the value that triggered the overflow or underflow condition. Until the counter is no longer in the overflow or underflow condition, it is not possible to clear the associated interrupt flag.</p>
<b>Workaround</b>
<p>Short of disabling the relevant interrupts, the simplest workaround is to manually increment or decrement TIMER_CNT so that the overflow or underflow condition no longer exists. Insert the following or similar code in the interrupt handler for the timer in question (TIMER0 in this case) to do this:</p>
<pre>uint32 intFlags = TIMER_IntGet(TIMER0);  if (intFlags &amp; TIMER_IEN_OF)     TIMER0-&gt;CNT += 1;  if (intFlags &amp; TIMER_IEN_UF)     TIMER0-&gt;CNT -= 1;</pre>
<p>It may be necessary for firmware to account for this adjustment in calculations that include the counter value.</p>
<b>Resolution</b>
<p>There is currently no resolution for this issue.</p>

### 3. Revision History

#### Revision 0.1

September, 2019

- Initial release.

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