# SiWT917 RCP Single Chip Wi-Fi® and Bluetooth® LE Wireless Solutions

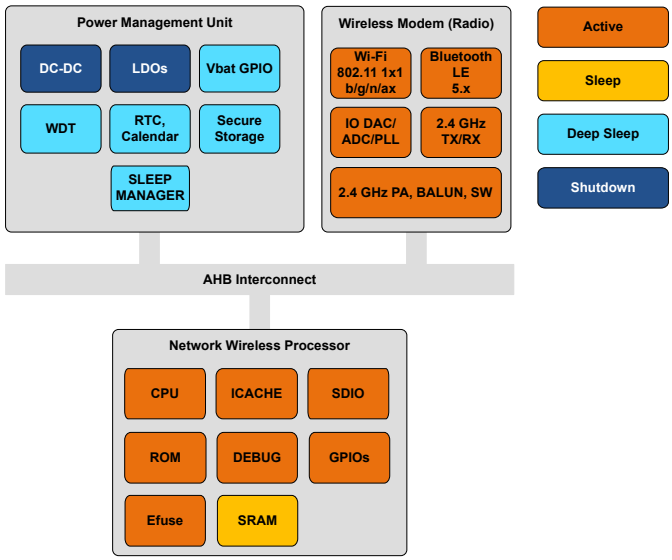
Silicon Labs' SiWT917 Radio Co-processor (RCP) is a comprehensive multi-protocol wireless sub-system. It has an integrated built-in wireless subsystem and power-management. It has a multi-threaded Network Wireless Processor (NWP) running up to 160 MHz. The wireless subsystem integrates baseband digital signal processing, analog front-end, calibration eFuse, 2.4 GHz RF transceiver and integrated power amplifier thus providing a fully-integrated solution for a range of hosted wireless applications.

SiWT917 applications include:

- Smart Home
- Security Cameras
- HVAC
- Smart Appliances
- Health and Fitness
- Pet Tracker
- Smart Cities
- Smart Meters
- Industrial Wearable
- Smart Buildings
- Smart hospitals

**KEY FEATURES**

- Wi-Fi 6 Single Band 2.4 GHz 20 MHz 1x1 stream IEEE 802.11 b/g/n/ax
- Bluetooth LE 5.4
- Wi-Fi 6 Benefits: TWT for improved efficiency and longer battery life, MU-MIMO/OFDMA for Higher Throughput, network capacity and low latency
- WLAN Tx power up to +19.5 dBm with integrated PA
- Bluetooth LE Tx power up to +19 dBm with integrated PA
- WLAN Rx sensitivity as low as -97.5 dBm
- Wi-Fi Standby Associated mode current: 65 µA @ 1-second beacon listen interval
- Operating temperature: -40 ºC to +85 ºC
- Single or dual-supply operation:
  - Single supply: 3.3 V
  - Dual supply: 3.3 V and 1.8 V



# 1. Feature List

- **Wi-Fi**
  - Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
  - Support for 20 MHz channel bandwidth for 802.11n and 802.11ax
  - Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi STA + BLE
  - Support for 802.11ax 20 MHz non-AP STA mandatory features (such as OFDMA, MU-MIMO) and optional features of individual Target wake-up time (iTWT), Broadcast TWT (bTWT)[2], Intra PPDU power save[2], SU extended range (ER), DCM (Dual Carrier Modulation). DL MU-MIMO, DL/UL OFDMA, MBSSID[2], BFRP, Spatial Re-use[2], BSS Coloring[2], and NDP feedback upto 4 antennas
  - Transmit power up to +19.5 dBm with integrated PA
  - Receive sensitivity as low as -97.5 dBm
  - Data Rates: 802.11b: 1, 2, 5.5, 11; 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps ; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
  - Operating Frequency Range: 2412 MHz – 2484 MHz
  - PTA Coexistence with Zigbee/Thread/Bluetooth
- **Intelligent Power Management**
  - Power optimizations leveraging multiple power domains and partitioned sub systems
  - Many system-, component-, and circuit-level innovations and optimizations
  - Different Power Modes
  - Deep sleep mode with only timer active
- **Bluetooth**
  - Transmit power up to +19 dBm with integrated PA
  - Receive sensitivity — LE 1 Mbps: -96 dBm, LR 125 kbps: -107 dBm
  - Operating Frequency Range — 2.402 GHz - 2.480 GHz
  - Support LE (1 Mbps & 2 Mbps) and LR (125 kbps & 500 kbps) rates
  - Advertising extensions
  - Data length extensions
  - LL privacy
  - LE dual role
  - BLE acceptlist
  - 2 Simultaneous BLE Connections (2 Peripheral, 2 Central, or 1 Central & 1 Peripheral)
- **RF Features**
  - Integrated baseband processor with calibration memory
  - Integrated RF transceiver, high-power amplifier, balun and T/R switch
- **Wireless Sub-System Power Consumption**
  - Wi-Fi 4 Standby Associated mode current: 65 µA @ 1-second beacon listen interval
  - Wi-Fi 1 Mbps Listen current: 16.5 mA
  - Wi-Fi LP chain Rx current: 22 mA
  - Deep Sleep current ~10 µA
- **Operating Conditions**
  - Single or dual-supply operation:
    - Single supply: 3.3 V
    - Dual supply: 3.3 V and 1.8 V
  - Operating temperature: -40 ºC to +85 ºC
- **Software and Regulatory Certifications** [1]
  - Wi-Fi Alliance: Wi-Fi 4, Wi-Fi 6
  - Bluetooth Qualification
  - Regulatory pre-certifications (FCC, IC, RED, UKCA, MIC)

**Note:**

1. For latest certification information, refer to regulatory app notes or contact Silicon Labs for availability.
2. For information about software roadmap features, and lists of available features and profiles, contact Silicon Labs or refer to Release Notes and Reference Manuals.

## 2. Ordering Information

**Table 2.1. List of OPNs**

| Part Number | Common Features | Device Type | Temperature |
|---|---|---|---|
| SiWT917M100XGTBA | Wi-Fi 6 Ultra low power IC, 7x7 DR-QFN, Integrated 2.4 GHz Radio | RCP | -40 to 85 ºC |

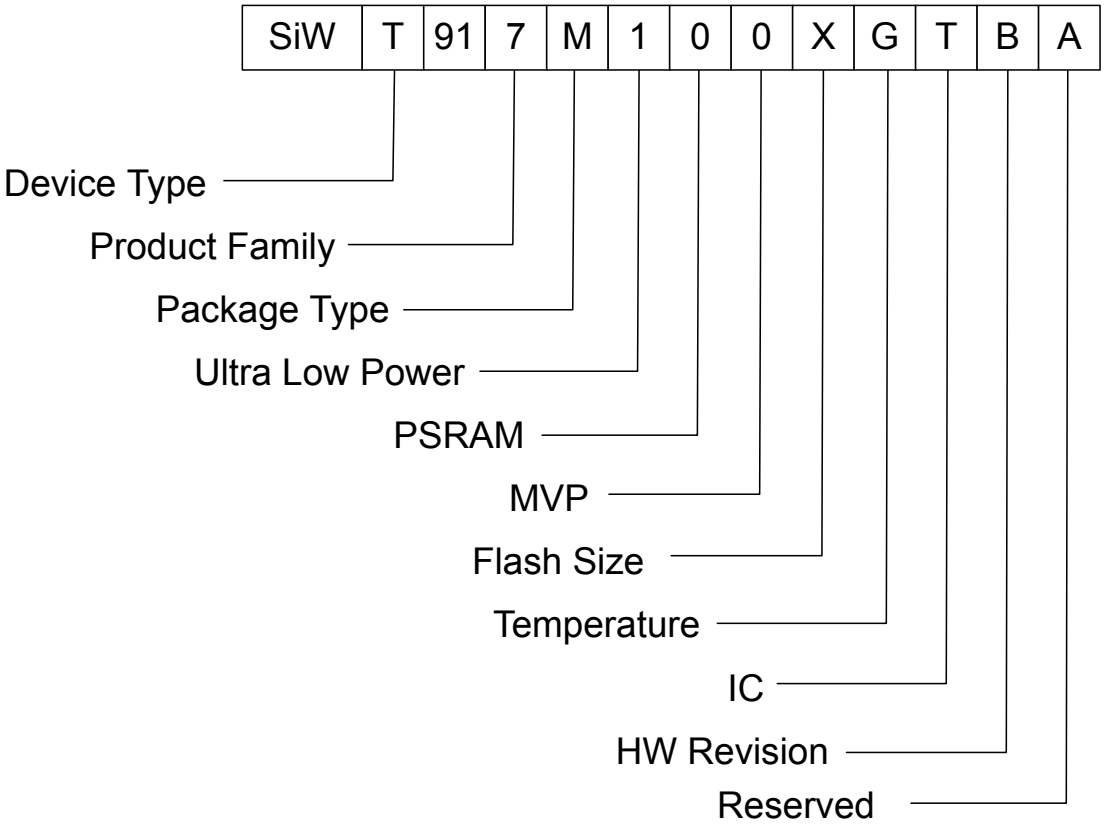



**Figure 2.1. Ordering Guide**

**Table 2.2. OPN Decoder**

| Field | Options |
|---|---|
| Device Type | **T**: RCP (Transceiver)<br>**N**: NCP<br>**G**: SoC |
| Product Family | **7**: Ultra-low power<br>**5**: Ultra-low cost |
| Package Type | **M**: DR-QFN |
| Ultra Low Power | **0**: ULP Features disabled<br>**1**: ULP Features enabled |

| Field | Options |
|---|---|
| PSRAM | **0**: No PSRAM Support<br>**1**: External PSRAM<br>**2**: 2 MB In-Package PSRAM<br>**4**: 8 MB In-Package PSRAM |
| MVP | **0**: MVP Features disabled<br>**1**: MVP Features enabled |
| Flash Size | **X**: No In-Package Flash<br>**L**: 4 MB In-Package Flash<br>**M**: 8 MB In-Package Flash |
| Temperature | **G**: -40 ºC to 85 ºC |
| IC/Module | **T**: IC Package |
| HW Revision | **B**: Revision B |
| Reserved | **A**: Reserved |

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# 3. Applications

**Smart Home**

Smart Locks, Light Emitting Diode (LED) lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

**Other Consumer Applications**

Toys, Smart dispensers, Weighing scales, Fitness Monitors, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

**Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)**

Infusion pumps, Sensors/actuators in Manufacturing, Smart Meters, Automotive After-market, Security Cameras, Gateways, etc.

# 4. Block Diagrams

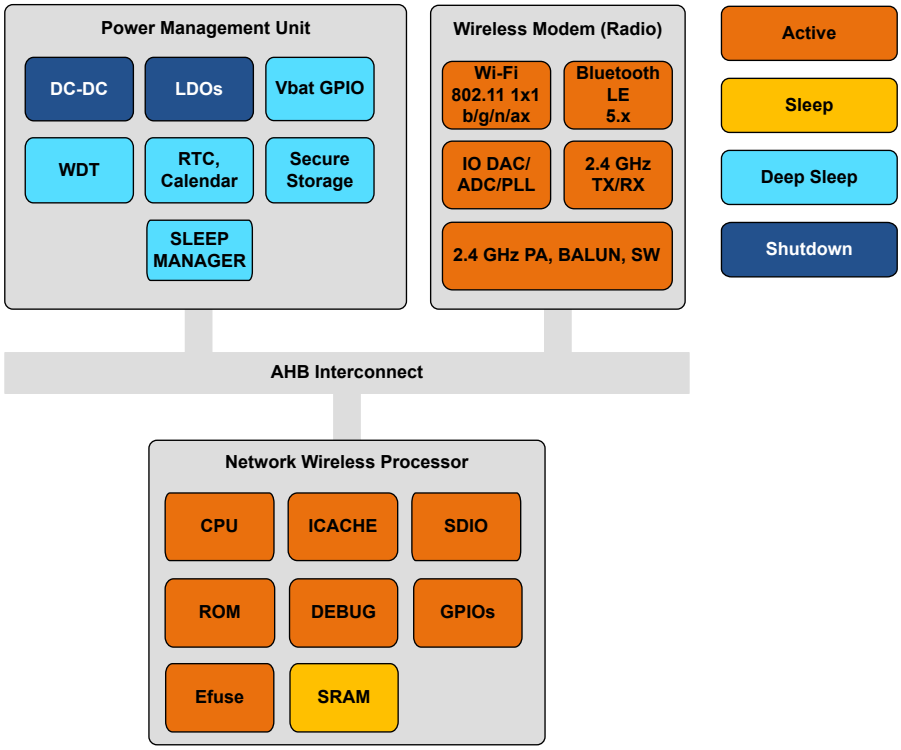


**Figure 4.1. System Block Diagram**

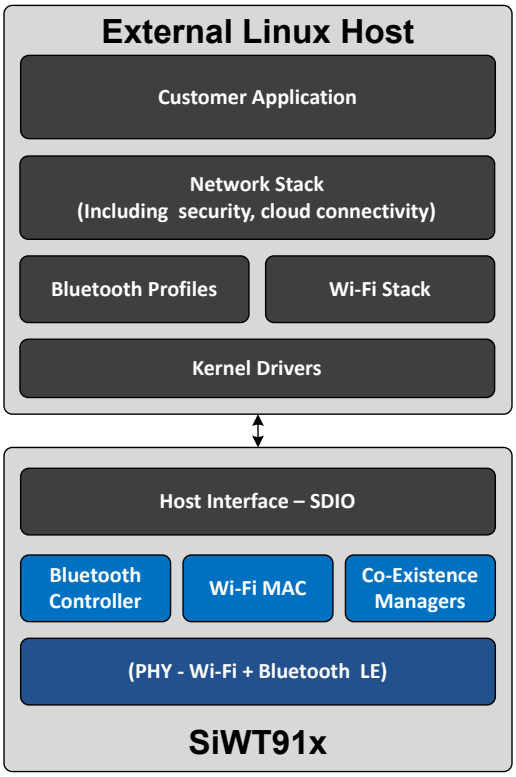


**Figure 4.2. SiWT917 RCP Software Architecture**

# 5. System Overview

## 5.1 Introduction

SiWT91x RCP includes a Network Wireless Processor (NWP) 4-Threaded processor running up to 160 MHz. The wireless subsystem has power, clocks/PLLs, bus-matrices, and memory to support transciever functionality with minimal external resources.

## 5.2 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
- Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
- Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi STA + BLE
- Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT),SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
- Integrated PA
- Data Rates—802.11b: up to 11 Mbps; 802.11g: up to 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
- Operating Frequency Range:  2412 MHz – 2484 MHz

### 5.2.1 MAC

- Conforms to IEEE 802.11b/g/n/j/ax standards for MAC
- Hardware accelerators for AES
- WPA, WPA2, WPA3 and WMM support
- AMPDU aggregation for high performance
- Firmware downloaded from host based on application

### 5.2.2 Baseband Processing

- Supports 11b: DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11ax, 802.11n: MCS 0 to MCS 7
- High-performance multipath handling in OFDM, DSSS, and CCK modes

## 5.3 Bluetooth

Key Features

- Transmit power up to +19.5 dBm with integrated PA
- Receive sensitivity — LE 1 Mbps: -96 dBm, LR 125 kbps: -107 dBm
- Operating Frequency Range — 2.402 GHz - 2.480 GHz
- Support LE (1 Mbps & 2 Mbps) and LR (125 kbps & 500 kbps) rates
- Advertising extensions
- Data length extensions
- LL privacy
- LE dual role
- BLE acceptlist
- Two simultaneous BLE connections (2 peripheral or 2 central, or 1 central and 1 peripheral)

### 5.3.1 MAC

**Link Manager**

- Creation, modification & release of physical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links

**Link Controller**

- Encodes and decodes header of BLE packets
- Manages flow control, acknowledgment, re-transmission requests, etc.
- Stores the last packet status for all physical transports
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

**Device Manager**

- Executes HCI Commands
- Controls Scan & Connection processes
- Controls all BLE Device operations except data transport operations
- BLE Controller state transition management
- Anchor point synchronization & management
- Scheduler

### 5.3.2 Baseband Processing

- Supports BLE 1 Mbps, 2 Mbps and long range 125 kbps, 500 kbps

## 5.4 RF Transceiver

- SiWT917 features two highly configurable RF transceivers supporting WLAN 11b/g/n/ax and Bluetooth LE wireless protocols. Both RF transceivers together operating in multiple modes covering High Performance (HP) and Low Power (LP) operations. List of operating modes are given in next section.
- It contains two fully integrated fractional-N frequency synthesizers having reference from internal oscillator with 40 MHz crystal. One of the synthesizer is a low power architecture which also caters single-bit data modulation feature for Bluetooth LE protocols.
- There are two transmitter chains in the chip. First one uses a direct conversion architecture getting carrier signal from the high-performance frequency synthesizer. It contains an on-chip balun and its output is terminated as single-ended output at “RF_TX” pin. This transmitter supports all the mentioned WLAN protocols, and Bluetooth LE protocol for high output power. The second transmitter is a low power architecture for supporting constant envelope modulation formats. This has two outputs differentiated by their maximum output power level. The 0 dBm output is shared with “RF_RX” pin and the 8 dBm output is terminated at “RF_BLETX” pin.
- The receiver contains two front end paths with a configurable common LNA catering HP and LP operations. This also has two analog base-band blocks where one is zero-IF architecture supporting all the mentioned WLAN protocols and the other one is low-IF architecture supporting Bluetooth LE. Input to the pin is “RF_RX” sharing with 0 dBm Tx output.
- Impedance matching for each RF pins need to be done separately for optimum performance.

### 5.4.1 Receiver and Transmitter Operating Modes

The available radio operating modes are

- WLAN HP TX - WLAN High-Performance Transmitter with up to 19.5 dBm PA
- WLAN HP RX - WLAN High-Performance Receiver
- WLAN LP RX - WLAN Low-Power Receiver
- BLE HP TX - Bluetooth LE High-Performance Transmitter with up to 19 dBm PA
- BLE HP RX - Bluetooth LE High-Performance Receiver
- BLE LP TX - Bluetooth LE Low-Power Transmitter with 8 dBm PA
- BLE LP TX - Bluetooth LE Low-Power Transmitter with 0 dBm PA
- BLE LP RX - Bluetooth LE Low-Power Receiver

**Note:** All the TX / RX modes are automatically controlled by radio firmware and not individually selectable.

## 5.5 Power Architecture

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/Shutdown).

### 5.5.1 Highlights

- Two integrated buck switching regulators (High performance and ULP) to enable efficient Voltage Scaling across wide operating mode currents ranging from <1 µA to 170 mA
- Multiple voltage domains with Independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/pads are inactive.
- Flexible switching between different Active states with controls from Software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default thereby reducing the power consumption in inactive state.
- Low wakeup times as configurable by Software.

### 5.5.2 System Power Supply Configurations

SiWT917 chipsets support highly flexible power supply configurations for various application scenarios. Two application scenarios are listed below.

- 3.3 V single supply - A single 3.3 V supply derived from the system PMU can be input to all I/O supplies.
- 1.8 V and 3.3 V supply - A 1.8 V supply derived from the system PMU can be input to all I/O supplies except PA2G_AVDD. A 3.3 V supply derived from system Power Management Unit (PMU) can be fed to the power amplifier supply pin PA2G_AVDD. There will be slight RF performance degradation if antenna select signals (ULP_GPIO_4, ULP_GPIO_5, ULP_GPIO_0) are powered at 1.8 V from the ULP_IO_VDD supply.

### 5.5.3 Power Management

The SiWT917 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.

- LC DC-DC switching converter for RF and digital blocks
  - Input voltage (1.8 V or 3.3 V) on pin VINBCKDC
  - Nominal Output - 1.45 V and 170 mA maximum load on pin VOUTBCKDC
- SC DC-DC - Switching converter for Always-ON core logic domain
  - Input voltage (1.8 V or 3.3 V) on pin UULP_VBATT_1 and UULP_VBATT_2
  - Nominal Outputs
    - 1.05 V on pin UULP_VOUTSCDC
    - 0.75 V on pin UULP_VOUTSCDC_RETN
- SoC LDO - Linear regulator for digital blocks
  - Input - 1.45 V from LC DC-DC or external regulated supply on pin VINLDOSOC
  - Nominal Output - 1.15 V and 100 mA maximum load on pin VOUTLDOSOC
- LDO RF and AFE - Linear regulator for RF and AFE
  - Input - 1.45 V from LC DC-DC or external regulated supply on pin RF_AVDD
  - Nominal Output - 1.21 V on pin VOUTLDOAFE

  **Note:** Output of VOUTLDOAFE will be 0.75 V - 1.05 V after initial power-up, until the RF has been initialized.

- 1.8 V LDO - Linear 1.8 V regulator
  - Input voltage (1.8 V or 3.3 V) on pin VINLDO1P8
  - Nominal Output - 1.8 V and 48 mA maximum load on pin VOUTLDO1P8

## 5.6 Memory Architecture

There are on chip Read Only Memory (ROM) and Random Access Memory (RAM).

The NWP processor has the following memory:

- Embedded SRAM up to 672 KB total
- 448 KB of ROM
- 16 KB of Instruction cache (I cache)
- eFuse of 1024 bytes (used to store primary boot configuration and calibration parameters)

# 6. Pinout and Pin Description

## 6.1 Pin Diagram

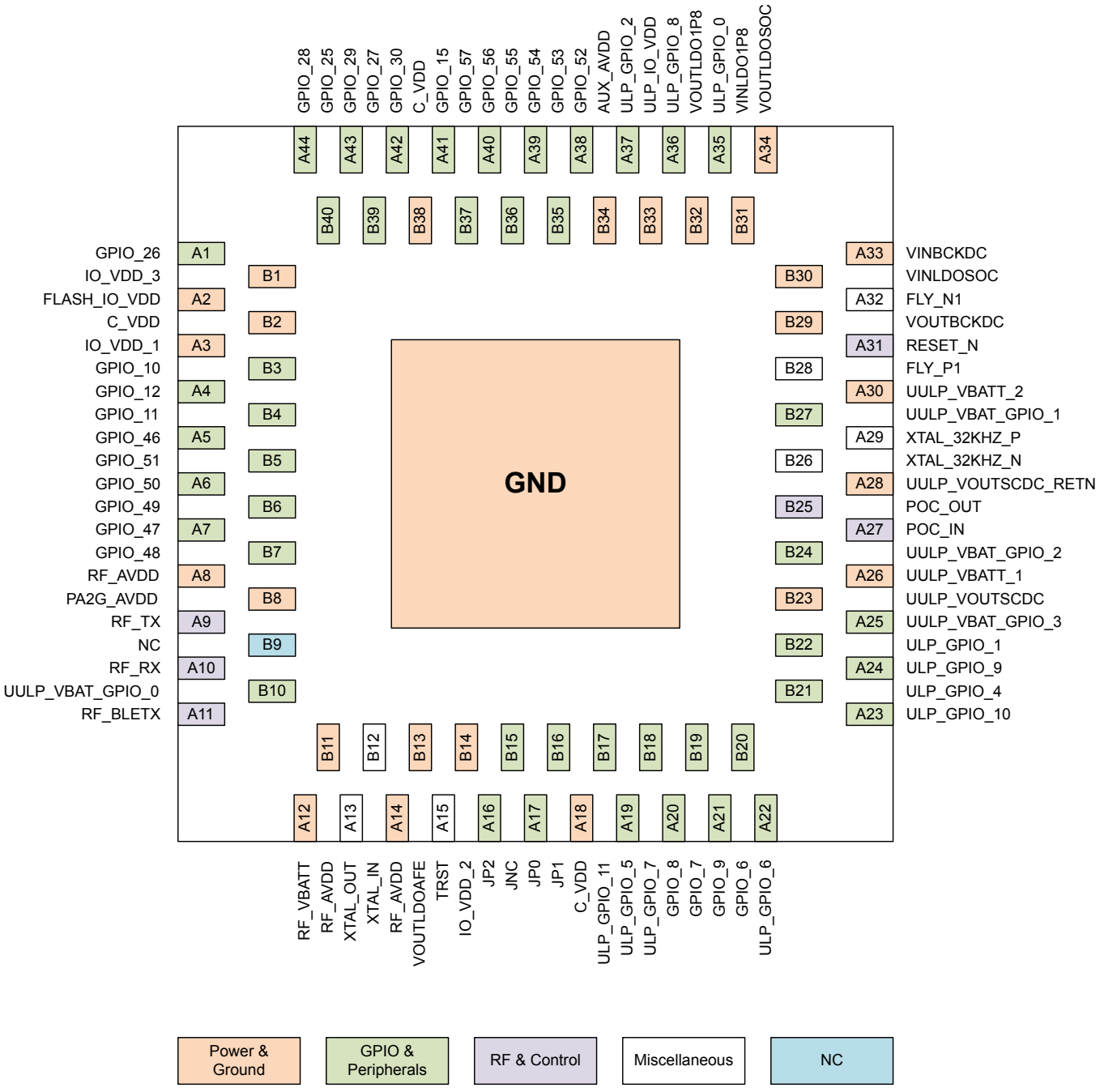


**Figure 6.1. SiWT917xxxxxxxBA**

## 6.2 Pin Description

### 6.2.1 RF and Control Interfaces

**Table 6.1. Chip Packages - RF and Control Interfaces**

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description |
|---|---|---|---|---|---|
| RF_TX | A9 | PA2G_AVDD | Output | NA | 2.4 GHz High Performance RF Output |
| RF_RX | A10 | RF_AVDD | Inout | NA | 2.4 GHz RF Input for High Performance WLAN and High Performance BLE. It can also be used as 2.4 GHz RF output for Low Power BLE 0 dBm |
| RF_BLETX | A11 | RF_AVDD | Output | NA | 2.4 GHz RF Output for Low Power BLE 8 dBm |
| RESET_N | A31 | UULP_VBATT_2 | Inout | NA | Active-low asynchronous reset signal, which resets only digital blocks. RESET_N will be pulled low if POC_IN is low. |
| POC_IN | A27 | UULP_VBATT_1 | Input | NA | This is an input to the chip which resets all analog and digital blocks in the device. It should be made high only after supplies are valid to ensure the IC is in safe state until valid power supply is available. |
| POC_OUT | B25 | UULP_VBATT_1 | Output | NA | This is internally generated. Initially, it is low. But it becomes high when the supplies (UULP_VBATT_1, UULP_VOUTSCDC) are valid. |
| ULP_GPIO_0 | A35 | ULP_IO_VDD | Inout | NA | Antenna select pin for External switch configuration. Please refer to Reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions. |
| ULP_GPIO_4 | B21 | ULP_IO_VDD | Inout | NA | Antenna select pin for External switch configuration. Please refer to Reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions. |
| ULP_GPIO_5 | A19 | ULP_IO_VDD | Inout | NA | Antenna select pin for External switch configuration. Please refer to Reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions. |

### 6.2.2 Power and Ground Pins

**Table 6.2. Chip Packages - Power and Ground Pins**

| Pin Name | Type | Pin Number | Direction | Description |
|---|---|---|---|---|
| UULP_VBATT_1 | Power | A26 | Input | Always-on VBATT Power supply to the UULP domains. |
| UULP_VBATT_2 | Power | A30 | Input | Always-on VBATT Power supply to the UULP domains. |
| RF_VBATT | Power | A12 | Input | Always-on VBATT Power supply to the RF. |
| VINBCKDC | Power | A33 | Input | Power supply for the on-chip buck DC-DC. |
| VOUTBCKDC | Power | B29 | Output | Output of the on-chip buck DC-DC. |
| VINLDOSOC | Power | B30 | Input | Power supply for SoC LDO. Connect to VOUTBCKDC as per the Reference Schematics. |
| VOUTLDOSOC | Power | A34 | Output | Output of SoC LDO. |
| VINLDO1P8 | Power | B31 | Input | Power supply for 1.8 V LDO |
| VOUTLDO1P8 | Power | B32 | Output | Output of 1.8 V LDO. |
| VOUTLDOAFE | Power | B13 | Output | Output of RF AFE LDO. |
| FLASH_IO_VDD | Power | A2 | Input | Unused for RCP device. Connect to VOUTLDO1P8. |
| IO_VDD_1 | Power | A3 | Input | I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| IO_VDD_2 | Power | B14 | Input | I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| IO_VDD_3 (SDIO_IO_VDD) | Power | B1 | Input | I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| ULP_IO_VDD | Power | B33 | Input | I/O Supply for ULP GPIOs. |
| PA2G_AVDD | Power | B8 | Input | Power supply for the 2.4 GHz RF Power Amplifier. |
| RF_AVDD | Power | A8, A14, B11 | Input | Power supply for the 2.4 GHz RF and AFE. Connect to VOUTBCKDC as per the Reference Schematics. |
| AUX_AVDD | Power | B34 | Output | Auxiliary LDO Output supply for the Analog peripherals. |
| UULP_VOUTSCDC | Power | B23 | Output | UULP Switched Cap DCDC Output. |
| UULP_VOUTSCDC_RETN | Power | A28 | Output | UULP Retention Supply Output. |
| C_VDD | Power | B2, A18, B38 | Input | Power supply for the digital core. Connect to the VOUTLDOSOC as per the Reference Schematics. |
| GND | Ground | GND Paddle | GND | Common ground pins. |

### 6.2.3 Peripheral Interfaces

**Table 6.3. Chip Packages - Peripheral Interfaces**

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| GPIO_6 | B20 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_7 | B19 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following.<br>PTA_GRANT: "PTA Grant" output signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. |
| GPIO_8 | A20 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_9 | A21 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_10 | B3 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_11 | B4 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep:** HighZ<br>This pin can be configured by software to be any of the following.<br>• WAKEUP_FROM_DEV: Used as a wakeup indication to host from device.<br>• It is part of Wake-on-Wireless functionality. It is recommended that one use an external weak pull-down resistor on this pin and software has to be configured suitably.<br>• Please check with Silabs for availability of this functionality. |
| GPIO_12 | A4 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_15 | A41 | IO_VDD_3 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| GPIO_25/SDIO_CLK | B40 | IO_VDD_3 | Inout | HighZ | Host: Default: Sleep; SDIO: SDIO_CLK - SDIO interface clock: HighZ; Non SDIO: HighZ: HighZ |
| GPIO_26/SDIO_CMD | A1 | IO_VDD_3 | Inout | HighZ | Host: Default: Sleep; SDIO: SDIO_CMD - SDIO interface CMD signal: HighZ; Non SDIO: HighZ: HighZ |
| GPIO_27/SDIO_D0 | B39 | IO_VDD_3 | Inout | HighZ | Host: Default: Sleep; SDIO: SDIO_D0 - SDIO interface Data0 signal: HighZ; Non SDIO: HighZ: HighZ |
| GPIO_28/SDIO_D1 | A44 | IO_VDD_3 | Inout | HighZ | Host: Default: Sleep; SDIO: SDIO_D1 - SDIO interface Data1 signal: HighZ; Non SDIO: HighZ: HighZ |
| GPIO_29/SDIO_D2 | A43 | IO_VDD_3 | Inout | HighZ | Host: Default: Sleep; SDIO: SDIO_D2 - SDIO interface Data2 signal: HighZ; Non SDIO: HighZ: HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| GPIO_30/SDIO_D3 | A42 | IO_VDD_3 | Inout | Pullup | <table><tr><td>Host</td><td>Default</td><td>Sleep</td></tr><tr><td>SDIO</td><td>SDIO_D3 - SDIO interface Data3 signal</td><td>HighZ</td></tr><tr><td>Non SDIO</td><td>HighZ</td><td>HighZ</td></tr></table> |
| GPIO_46 | A5 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_47 | A7 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_48 | B7 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_49 | B6 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_50 | A6 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_51 | B5 | IO_VDD_1 | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| GPIO_52 | A38 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_53 | B35 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_54 | A39 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_55 | B36 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_56 | A40 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_57 | B37 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_0 | A35 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>Antenna select pin for external switch configuration. Please refer to reference schematics for more info. |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| ULP_GPIO_1 | B22 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• PTA_REQ: "PTA Request" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. |
| ULP_GPIO_2 | A37 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_4 | B21 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>Antenna select pin for external switch configuration. Please refer to reference schematics for more info. |
| ULP_GPIO_5 | A19 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>Antenna select pin for external switch configuration. Please refer to reference schematics for more info. |
| ULP_GPIO_6 | A22 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following.<br>• PTA_PRIO: "PTA Priority" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. |
| ULP_GPIO_7 | B18 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_8 | A36 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_9 | A24 | ULP_IO_VDD | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_10 | A23 | ULP_IO_VDD | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_11 | B17 | ULP_IO_VDD | Inout | HighZ | **Default:**HighZ<br>**Sleep**: HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| UULP_VBAT_GPIO_0 | B10 | UULP_VBATT_1 | Output | High | **Default:** High<br>**Sleep:** High<br>This pin can be configured by software to be any of the following.<br>• SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode. |
| UULP_VBAT_GPIO_1 | B27 | UULP_VBATT_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep:** HighZ<br>UULP_VBAT_GPIO_1: Reserved |
| UULP_VBAT_GPIO_2 | B24 | UULP_VBATT_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep:** ULP_WAKEUP<br>• After bootloading, this signal is an active-high input to indicate that the device should wakeup from its Ultra Low Power (ULP) sleep mode. |
| UULP_VBAT_GPIO_3 | A25 | UULP_VBATT_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep:** HighZ<br>Reserved |
| JP0 | A17 | IO_VDD_2 | Input | Pullup | **Default:** JP0<br>**Sleep**: HighZ<br>JP0 - Reserved. Connect to a test point for debugging purposes |
| JP1 | B16 | IO_VDD_2 | Input | Pullup | **Default:** JP1<br>**Sleep**: HighZ<br>JP1 - Reserved. Connect to a test point for debugging purposes |
| JP2 | A16 | IO_VDD_2 | Input | Pullup | **Default:** JP2<br>**Sleep**: HighZ<br>JP2 - Reserved. Connect to a test point for debugging purposes |
| JNC | B15 | IO_VDD_2 | Output | Pullup | **Default:** JNC<br>**Sleep**: HighZ<br>JNC - Reserved. Connect to a test point for debugging purposes |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|

**Note:**

1. "Default" state refers to the state of the device after initial boot loading and firmware loading is complete.
2. "Sleep" state refers to the state of the device after entering Sleep state
3. Please refer to "Hardware Reference Manual" for software programming information
4. Please refer to "Software Reference Manual" for software programming information
5. In the application, wherever SiWT917 is connected to an external host, during the power-off state, the host should ensure that all the pins (analog or digital) connected to the SiWT917 are not driven. Else, the pins must be grounded.

### 6.2.4 Miscellaneous Pins

**Table 6.4. Miscellaneous Pins**

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description |
|---|---|---|---|---|---|
| FLY_P1 | B28 | NA | Input | NA | Fly Capacitor for Switched cap DCDC. Please refer to Reference Schematics |
| FLY_N1 | A32 | NA | Input | NA | Fly Capacitor for Switched cap DCDC. Please refer to Reference Schematics |
| XTAL_IN | B12 | RF_VBATT | Input | NA | Input to the on-chip oscillator from the external 40 MHz crystal. |
| XTAL_OUT | A13 | RF_VBATT | Output | NA | Output of the on-chip oscillator to the external 40 MHz crystal. |
| TRST | A15 | IO_VDD_2 | Input | HighZ | Test signal. Connect to Ground. |
| XTAL_32KHZ_N | B26 | NA | Inout | NA | Analog Pin. 32.768 kHz crystal connection |
| XTAL_32KHZ_P | A29 | NA | Inout | NA | Analog Pin. 32.768 kHz crystal connection |
| NC | B9 | NA | NA | NA | No-Connect |

# 7. Electrical Specifications

## 7.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at https://www.silabs.com/about-us/quality.

**Note:** All the specifications are preliminary and subject to change.

**Table 7.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature | $T_{store}$ | | -40 | — | 125 | °C |
| Maximum junction temperature | $T_{j\_max}$ | | — | — | 125 | °C |
| Always-on VBATT supply to the UULP Domains | $V_{UULP\_VBATT\_1}$ | | -0.5 | — | 3.63 | V |
| Always-on VBATT supply to the UULP Domains | $V_{UULP\_VBATT\_2}$ | | -0.5 | — | 3.63 | V |
| Always-on VBATT Power supply to the RF | $V_{RF\_VBATT}$ | | -0.5 | — | 3.63 | V |
| Power supply for the on-chip Buck | $V_{VINBCKDC}$ | | -0.5 | — | 3.63 | V |
| Power supply for SoC LDO | $V_{VINLDOSOC}$ | | -0.5 | — | 1.8 | V |
| Power supply for 1.8 V LDO | $V_{VINLDO1P8}$ | | -0.5 | — | 3.63 | V |
| I/O supply for Flash | $V_{FLASH\_IO\_VDD}$ | | -0.5 | — | 3.63 | V |
| I/O supplies for GPIOs | $V_{IO\_VDD\_1}$ | | -0.5 | — | 3.63 | V |
| I/O supplies for GPIOs | $V_{IO\_VDD\_2}$ | | -0.5 | — | 3.63 | V |
| I/O supplies for GPIOs | $V_{IO\_VDD\_3}$ | | -0.5 | — | 3.63 | V |
| I/O supplies for ULP GPIOs | $V_{ULP\_IO\_VDD}$ | | -0.5 | — | 3.63 | V |
| DC voltage on any I/O pin [1] | $V_{IO\_PIN}$ | | -0.5 | — | VDD + 0.5 | V |
| Current per I/O pin | $I_{IOMAX}$ | Sink | — | — | 100 | mA |
| | | Source | — | — | 100 | mA |
| Power supply for the 2.4 GHz RF Power Amplifier | $V_{PA2G\_AVDD}$ | | -0.5 | — | 3.63 | V |
| Power supply for the 2.4 GHz RF and AFE | $V_{RF\_AVDD}$ | | -0.5 | — | 1.98 | V |
| Power supply for the digital core | $V_{C\_VDD}$ | | -0.5 | — | 1.21 | V |
| Total average max current into chip | $I_{Pmax}$ | | — | — | 500 | mA |

**Note:**
1. VDD = I/O supply domain pin. Refer to pin description tables for supply domain associated with each I/O.

## 7.2 Recommended Operating Conditions

**Note:** The device may operate continuously at the maximum allowable ambient $T_{ambient}$ rating as long as the maximum junction $T_{junction(max)}$ is not exceeded. For an application with significant power dissipation, the allowable $T_{ambient}$ may be lower than the maximum $T_{ambient}$ rating. $T_{ambient} = T_{junction(max)} - (\Theta_{JA} \times \text{Power Dissipation})$. Refer to the Thermal Characteristics table for $\Theta_{JA}$.

**Table 7.2. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient temperature | $T_{ambient}$ | | -40 | 25 | 85 | °C |
| Junction temperature | $T_{junction}$ | | — | — | 105 | °C |
| Power supply for UULP_VBATT_1, UULP_VBATT_2, and RF_VBATT [1] | $V_{VBATT}$ | 3.3 V nominal operation | 2.97 | 3.3 | 3.63 | V |
| | | 1.8 V nominal operation | 1.71 | 1.8 | 1.98 | V |
| Power supply for the on-chip Buck [1] | $V_{VINBCKDC}$ | 3.3 V nominal operation | 2.97 | 3.3 | 3.63 | V |
| | | 1.8 V nominal operation | 1.71 | 1.8 | 1.98 | V |
| Power supply for 1.8 V LDO [1] | $V_{VINLDO1P8}$ | Regulation mode | 2.97 | 3.3 | 3.63 | V |
| | | Bypass mode | 1.71 | 1.8 | 1.98 | V |
| Power supply for SoC LDO | $V_{VINLDOSOC}$ | | 1.35 | 1.45 | 1.55 | V |
| I/O supply for Flash | $V_{FLASH\_IO\_VDD}$ | | 1.71 | 1.8 | 1.98 | V |
| Power supply for the 2.4 GHz RF Power Amplifier | $V_{PA2G\_AVDD}$ | | 2.97 | 3.3 | 3.63 | V |
| Power supply for IO_VDD_1 [1] | $V_{IO\_VDD\_1}$ | 3.3 V nominal operation | 2.97 | 3.3 | 3.63 | V |
| | | 1.8 V nominal operation | 1.71 | 1.8 | 1.98 | V |
| Power supply for IO_VDD_2 [1] | $V_{IO\_VDD\_2}$ | 3.3 V nominal operation | 2.97 | 3.3 | 3.63 | V |
| | | 1.8 V nominal operation | 1.71 | 1.8 | 1.98 | V |
| Power supply for IO_VDD_3 [1] | $V_{IO\_VDD\_3}$ | 3.3 V nominal operation | 2.97 | 3.3 | 3.63 | V |
| | | 1.8 V nominal operation | 1.71 | 1.8 | 1.98 | V |
| Power supply for ULP_IO_VDD [1] | $V_{ULP\_IO\_VDD}$ | 3.3 V nominal operation | 2.97 | 3.3 | 3.63 | V |
| | | 1.8 V nominal operation | 1.71 | 1.8 | 1.98 | V |

**Note:**

1. Supplies can operate at a nominal 3.3 V or 1.8 V level independent of the other supplies in the system.

## 7.3 DC Characteristics

### 7.3.1 RESET_N and POC_IN Pins

**Table 7.3. RESET_N and POC_IN Pins**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | RESET_N pin, UULP_VBATT_2 = 3.3 V | 0.8 * UULP_VBATT_2 | — | — | V |
| | | RESET_N pin, UULP_VBATT_2 = 1.8 V | 1.17 | — | — | V |
| | | POC_IN pin, UULP_VBATT_1 = 3.3 V | 2.76 | — | — | V |
| | | POC_IN pin, UULP_VBATT_1 = 1.8 V | 1.38 | — | — | V |
| Low level input voltage | $V_{IL}$ | RESET_N pin, UULP_VBATT_2 = 3.3 V | — | — | 0.3 * UULP_VBATT_2 | V |
| | | RESET_N pin, UULP_VBATT_2 = 1.8 V | — | — | 0.63 | V |
| | | POC_IN pin, UULP_VBATT_1 = 3.3 V | — | — | 1.10 | V |
| | | POC_IN pin, UULP_VBATT_1 = 1.8 V | — | — | 0.24 | V |

### 7.3.2 Power On Control (POC) and Reset

There are three signals involved in power-on control and reset of the device:

- POC_IN: When pulled low, POC_IN will reset all of the internal blocks in the device. The POC_IN signal can be controlled either by external circuitry, by POC_OUT, or both.
- RESET_N: RESET_N is an open-drain signal which will be pulled low during a chip reset. It is released after POC_IN is high. RESET_N should be connected to an RC circuit to fulfill the timing requirements shown in Figure 7.1 Power Up Sequence on page 26.
- POC_OUT: The POC_OUT signal is the output of the internal blackout supply monitor. POC_OUT is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to place the IC in a safe state until a valid supply is available for proper operation. During power up, POC_OUT stays low until the UULP_VBATT_1 reaches 1.6 V. After the VBATT supply exceeds 1.6 V, POC_OUT becomes high and normal operation begins. If VBATT becomes lower than the blackout threshold voltage, POC_OUT will return low. POC_OUT can be used to provide chip reset by connecting to POC_IN in a loopback configuration.

The recommended schematic for the reset signals is shown in 8.1 Schematics.

Figure 7.1 Power Up Sequence on page 26 shows the signal timing when POC_OUT, POC_IN, and RESET_N are connected per the recommended schematic. The POC_IN-to-RESET_N delay will occur when POC_IN transitions from low to high. VBATT in the figure refers to the connection of UULP_VBATT_1 and UULP_VBATT_2 (connected together in the schematic).

In this configuration the system only has to control the supply (VBATT) during power-up and power down and need not control POC_IN externally. On power-up the chip will be reset internally. The power-down sequence will follow VBATT and external control of POC_IN is not required.

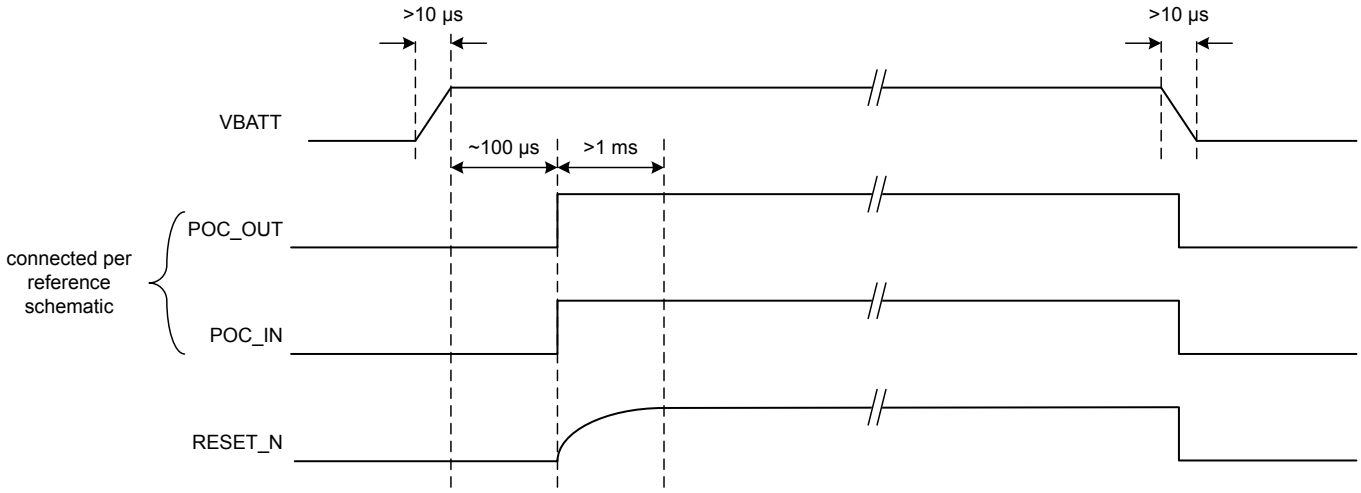


**Figure 7.1. Power Up Sequence**

If the chip is to be reset from an external host device while powered up, the POC_IN signal should be pulled low for at least 10 ms as shown in Figure 7.2 External Reset via POC_IN on page 27. Upon release of POC_IN, the POC_IN-to-RESET_N delay will occur.

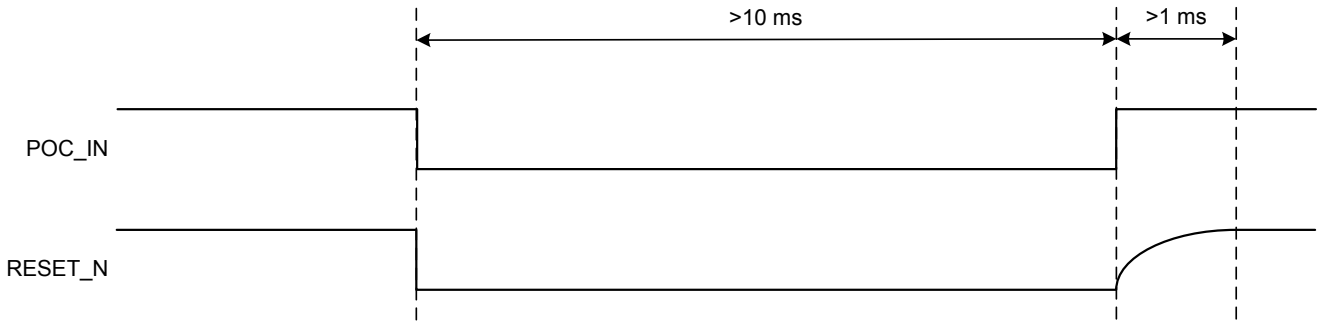


**Figure 7.2. External Reset via POC_IN**

In the above timing diagrams, it is assumed that all supplies including VBATT are connected together. If they are not connected together and independently controlled, then the guidance below must be followed.

- **Case1**: POC is looped back and there is no external control for POC_IN
  - All supplies can be enabled at the same time, if possible
  - If supplies cannot be enabled at the same time, the VBATT supplies should be powered up first and all other supplies should be powered on at least 1 ms before RESET_N is high. The RC circuit controlling RESET_N must be adjusted to provide the appropriate delay.
  - While powering down, supplies can be powered off simultaneously, or with VBATT the last to be disabled.
- **Case2**: POC is looped back and there is external control for POC_IN during power-up / power-down.
  - All supplies can be enabled at the same time, or VBATT may be enabled before other supplies.
  - POC_IN should be kept low for at least 600 us after all the supplies have settled.
  - On power-down, POC_IN can be driven low before disabling the supplies. Supplies can be powered off simultaneously, or with VBATT the last to be disabled.

### 7.3.3 ULP Regulators

ULP (Ultra Low Power) regulators are used to power low power Always-ON digital and analog power management circuitry inside the IC. The ULP regulators include two high power LDOs, a Low power LDO, and a switched capacitor DC-DC regulator. These regulators operate directly off of UULP_VBATT_2.

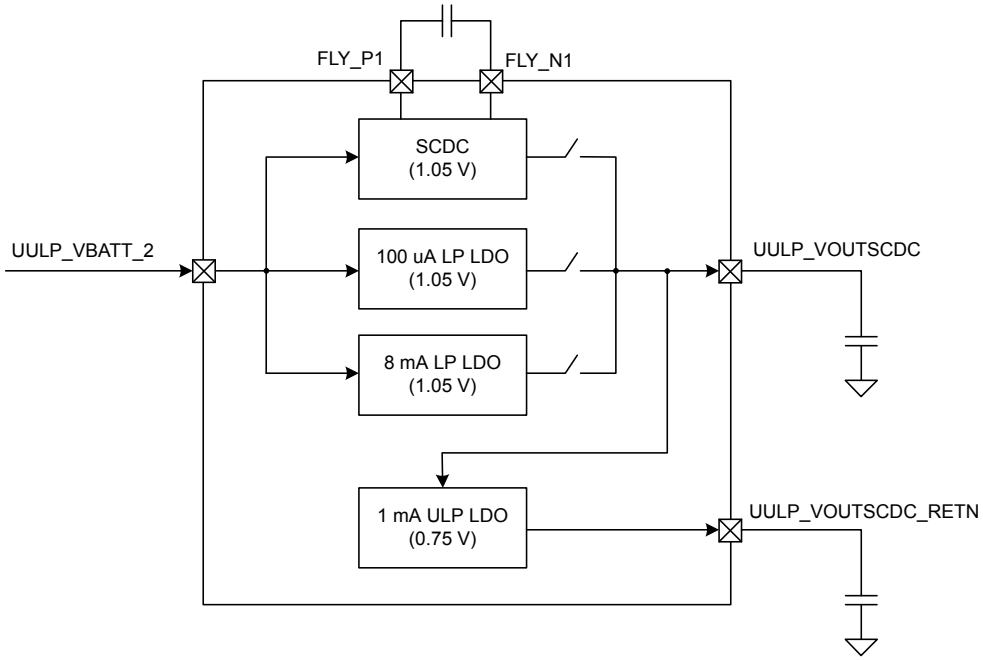


**Figure 7.3. Block Diagram**

#### 7.3.3.1 SC-DCDC

SC-DCDC stands for a Switched Capacitor DC-DC regulator. It operates from UULP_VBATT_2 and generates a programmable output voltage. It has two major modes of operation, viz. LDO mode and DC-DC mode. And further each of these modes have a low power and high power option.

The IC starts up in the LDO mode and later switches to DC-DC Mode.

**Table 7.4. SC-DCDC - Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range [1] | $V_{IN}$ | | 1.71 | — | 3.63 | V |
| Output Voltage at UULP_VOUTSCDC | $V_{OUTSCDC}$ | | — | 1.05 | — | V |
| Output Voltage at UULP_VOUTSCDC_RETN | $V_{OUTRETN}$ | | — | 0.75 | — | V |

**Note:**
1. The ULP regulator switches from SC-DCDC mode to LDO mode for $V_{in}$ lower than 2.4 V

### 7.3.4 Power Management Unit

This section describes and specifies the Power Management Unit solution for the mixed signal System on Chip (SoC).

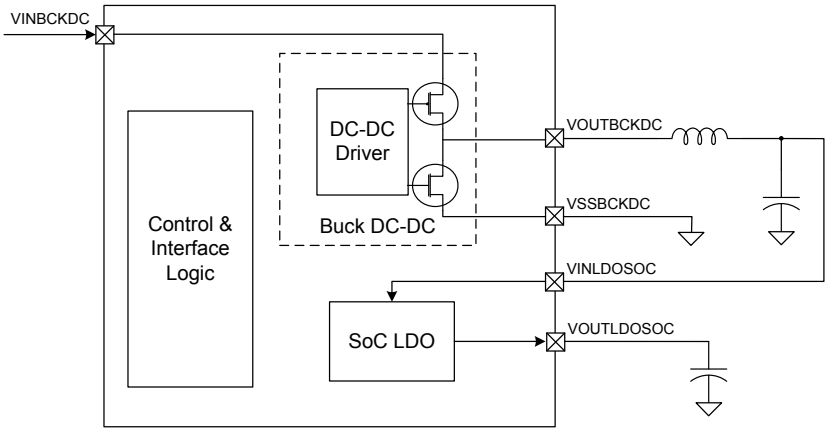


**Figure 7.4. Power Management Block Diagram**

**Power Management Unit**

The major features are

- 1.45 V DCDC switching converter
- 1.15 V LDO for SOC digital supply

#### 7.3.4.1 DCDC Switching Converter

- Power save mode at light load currents.
- 100% duty cycle for lowest dropout.
- Soft start

**Table 7.5. DCDC Switching Converter Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Supply Voltage (VINBCKDC) | $V_{in}$ | | 1.71 | 3.3 | 3.63 | V |
| Output Voltage Range (VOUTBCKDC) | $V_{out}$ | | 1.35 | 1.45 | 1.6 | V |
| Load current | $I_{load}$ | Active mode | — | — | 170 | mA |

#### 7.3.4.2 SoC LDO Electrical Specifications

**Table 7.6. SoC LDO Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Supply Voltage (VINLDOSOC) | $V_{in}$ | | 1.35 | 1.45 | 1.55 | V |
| Output Voltage Range (VOUTLDOSOC) | $V_{out}$ | | 1.05 | 1.15 | 1.20 | V |
| Load current | $I_{load}$ | | — | — | 100 | mA |

### 7.3.5 Thermal Characteristics

**Table 7.7. Thermal Characteristics**

| Package | Board | Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|---|---|
| 84 Pin DR-QFN (7 mm x 7 mm) | JEDEC - High Thermal Cond. (2s2p)[1] | Thermal Resistance, Junction to Ambient | $\Theta_{JA}$ | Still Air | 30 | °C/W |

**Note:**
1. PCB: 76.2 mm x 114.3 mm x 1.6 mm (JEDEC High Effective); 2s2p = 2 signals, 2 planes.
2. The absolute maximum device current when transmitting at highest transmit power will not exceed 400 mA.

### 7.3.6 Digital I/O Signals

**Table 7.8. Digital I/O Signals**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | IO_VDDx = 3.3 V | 2 | — | — | V |
| | | IO_VDDx = 1.8 V | 1.17 | — | — | V |
| Low level input voltage | $V_{IL}$ | IO_VDDx = 3.3 V | — | — | 0.8 | V |
| | | IO_VDDx = 1.8 V | — | — | 0.63 | V |
| Low level output voltage | $V_{OL}$ | | — | — | 0.4 | V |
| High level output voltage | $V_{OH}$ | | IO_VDDx - 0.4 | — | — | V |
| Low level output current | $I_{OL}$ | GPIO_* and ULP_GPIO_* pins | 2 | 4 | 12 | mA |
| | | UULP_GPIO_* | 1 | — | 2 | mA |
| High level output current | $I_{OH}$ | GPIO_* and ULP_GPIO_* pins | 2 | 4 | 12 | mA |
| | | UULP_GPIO_* | 1 | — | 2 | mA |

## 7.4 AC Characteristics

### 7.4.1 Clock Specifications

SiWT917 chipsets include the following clock options:

- Low frequency clock options for sleep manager and RTC
  - 32.768 kHz on-chip crystal oscillator for an external crystal at pins XTAL_32KHZ_P and XTAL_32KHZ_N. **Required for all power-sensitive Wi-Fi, BLE, and Coex use cases.**
  - Internal 32 kHz RC oscillator. Suitable only for applications with low timing accuracy requirements, and no critical timing. Typical accuracy is +/- 1.2%.
- High frequency clock options
  - 40 MHz on-chip crystal oscillator with external crystal at XTAL_IN and XTAL_OUT pins for RF reference
  - Internal RC oscillator, used during device boot-up
  - Internal high-frequency ring oscillator

#### 7.4.1.1 Low Frequency Clocks

Low-frequency clock selection can be done through software. The RC oscillator clock is not suited for high timing accuracy applications and may increase overall system current consumption in duty-cycled power modes.

**Table 7.9. 32 kHz RC Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillator Frequency | $f_{osc}$ | | — | 32 | — | kHz |
| Frequency variation across temperature | $f_{osc\_Acc}$ | | — | 1.2 | — | % |

**32.768 kHz Internal XTAL Oscillator**

There is an option to use internal 32.768 kHz low-frequency XTAL clock with a crystal attached to the XTAL_32KHZ_P and XTAL_32KHZ_N pins. Below are the recommended external crystal specs that need to connect to the internal xtal oscillator.

**Table 7.10. Internal 32.768 kHz XTAL Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillator Frequency [1] | $f_{osc}$ | | — | 32.768 | — | kHz |
| Drive Level | Drive | | 0.5 | — | — | uW |
| Frequency Variation with Temp and Voltage [2] | $f_{osc\_Acc}$ | | — | +/-250 | — | ppm |
| Equivalent series resistance | ESR | | — | — | 80 | kΩ |
| Load capacitance range | $C_L$ | | 4 | — | 12.5 | pF |

**Note:**

1. Oscillator specified for fundamental mode, parallel resonant crystal
2. Combined frequency offset must be below this limit, including temperature induced changes, tolerance, and the variance of load capacitances (load capacitor and parasitic trace impedance)

#### 7.4.1.2 40 MHz Clock

The 40 MHz internal oscillator mode can be used by connecting a 40 MHz crystal between the pins XTAL_P and XTAL_N. Load capacitance is integrated inside the chipset and calibrated and the calibrated value can be stored in eFuse using calibration software.

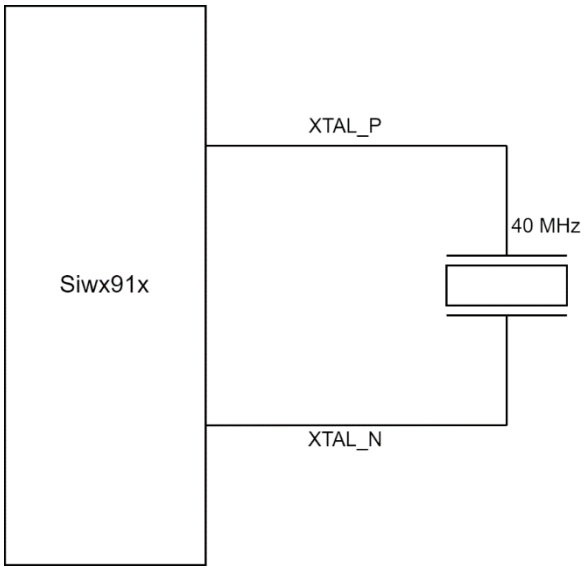


**Table 7.11. 40 MHz Crystal Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillator Frequency [1] | $f_{osc}$ | | — | 40 | — | MHz |
| Drive Level | Drive | | 100 | — | — | uW |
| Frequency Variation with Temp and Voltage | $f_{osc\_Acc}$ | | -20 | — | 20 | ppm |
| Equivalent series resistance | ESR | | — | — | 60 | Ω |
| Load capacitance range | $C_L$ | | 7 | — | 10 | pF |

**Note:**
1. Oscillator specified for fundamental mode, parallel resonant crystal

### 7.4.2 SDIO 2.0 Secondary

#### 7.4.2.1 Full Speed Mode

**Table 7.12. SDIO 2.0 Secondary Full Speed Mode**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SDIO_CLK | $f_{sdio\_clk}$ | | — | — | 25 | MHz |
| SDIO_DATA, SDIO_CMD input setup time | $t_s$ | | 4 | — | — | ns |
| SDIO_DATA, SDIO_CMD input hold time | $t_h$ | | 1.2 | — | — | ns |
| SDIO_DATA, clock to output delay | $t_{od}$ | | — | — | 13 | ns |
| Output Load | $C_L$ | | 5 | — | 10 | pF |

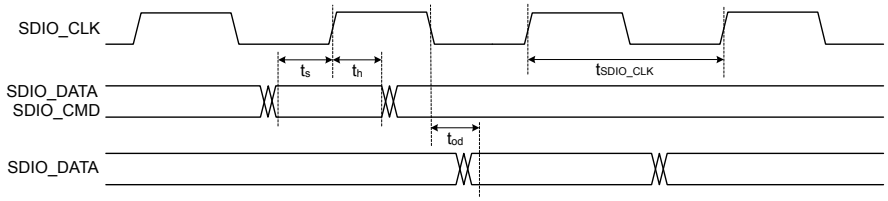


**Figure 7.5. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode**

#### 7.4.2.2 High Speed Mode

**Table 7.13. SDIO 2.0 Secondary High Speed Mode**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SDIO_CLK | $f_{sdio\_clk}$ | | 25 | — | 50 | MHz |
| SDIO_DATA, input setup time | $t_s$ | | 4 | — | — | ns |
| SDIO_DATA, input hold time | $t_h$ | | 1.2 | — | — | ns |
| SDIO_DATA, clock to output delay | $t_{od}$ | | 2.5 | — | 13 | ns |
| Output Load | $C_L$ | | 5 | — | 10 | pF |

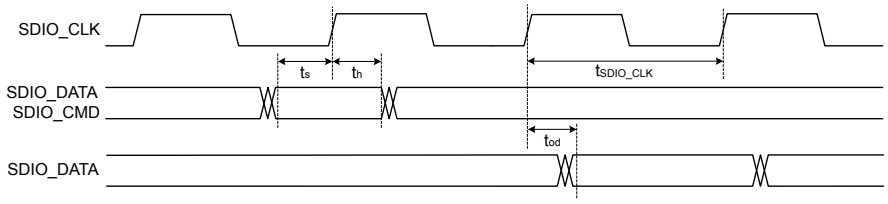


**Figure 7.6. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode**

### 7.4.3 GPIO Pins

**Table 7.14. GPIO Pins**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rise time | $t_{rf}$ | Pin configured as output | 1 | — | 5 | ns |
| Fall time | $t_{ff}$ | Pin configured as output | 0.9 | — | 5 | ns |
| Rise time | $t_r$ | Pin configured as input | 0.3 | — | 1.3 | ns |
| Fall time | $t_f$ | Pin configured as input | 0.2 | — | 1.2 | ns |

### 7.5 RF Characteristics

In the sub-sections below,

- All numbers are measured at $T_A$ = 25°C, PA2G_AVDD = VINBCKDC = 3.3 V using an external 40 MHz crystal, unless otherwise stated.
- Please refer to 8. Reference Schematics, BOM and Layout Guidelines. As shown in Figure 8.4 Option 1: RF Frontend with External Switch on page 52, there are three RF pins at the IC: RF_TX, RF_RX, and RF_BLETX. The RF front end for testing includes the matching network, RF switch and a band-pass filter. Typical front-end loss is about 2 dB. Silicon Labs recommends using the suggested reference design to meet these specs.
- All reported Receiver Sensitivity and Transmit Power numbers are based on the RF front end option shown in Figure 8.4 Option 1: RF Frontend with External Switch on page 52. The value at the antenna port (ANT1) will be based on front end loss, which is typically 2 dB lower than pins RF1, RF2, and RF3 of the RF switch (SW2). Using the internal switch option incurs 1-1.5 dBm performance degradation.
- Supported WLAN channels for different regions include:
  - US: Channels 1 (2412 MHz) through 11 (2462 MHz)
  - Europe: Channels 1 (2412 MHz) through 13 (2472 MHz)
  - Japan: Channels 1 (2412 MHz) through 14 (2484 MHz), Channel 14 supports 1 and 2 Mbps data rates only

### 7.5.1 WLAN 2.4 GHz Transmitter Characteristics

#### 7.5.1.1 WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_TX).

**Table 7.15. WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Power for 20 MHz Bandwidth, with EVM limits [1] [2] [3] | POUT | 802.11b 1 Mbps DSSS, EVM< -9 dB | — | 19 | — | dBm |
| | | 802.11b 11 Mbps CCK, EVM< -9 dB | — | 19 | — | dBm |
| | | 802.11g 6 Mbps OFDM, EVM< -5 dB [4] | — | 19.5 | — | dBm |
| | | 802.11g 54 Mbps OFDM, EVM< -25 dB [4] | — | 15.5 | — | dBm |
| | | 802.11n HT20 MCS0 Mixed Mode, EVM< -5 dB [4] | — | 19.5 | — | dBm |
| | | 802.11n HT20 MCS7 Mixed Mode, EVM< -27 dB [4] | — | 14.5 | — | dBm |
| | | 802.11ax HE20 MCS0 SU, EVM< -5 dB [5] [4] | — | 18.5 | — | dBm |
| | | 802.11ax HE20 MCS7 SU, EVM< -27 dB [5] [4] | — | 13 | — | dBm |
| Power variation across channels | $POUT_{VAR\_CH}$ | | — | 2 | — | dB |
| Power variation across temperature | $POUT_{VAR\_T}$ | -40 to +85 °C | — | 3 | — | dB |

**Note:**

1. Transmit power listed in this table is average power across all channels. Customers should calibrate crystal error and follow application note guildelines to achieve regulatory compliance.
2. TX power in edge channels will be limited by Restricted band edge in the FCC region.
3. Refer to the Wi-Fi Gain Table section in AN1437 for details on TX power backoff for compliance with regulatory limits.
4. 11b/g/n/ax @ Channels(1-13) TX power will be limited by antenna conducted output power test case (dBm/MHz) in MIC region.
5. 11ax TX power will be limited by PSD in the ETSI region.

### 7.5.2 WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin RF_RX

**Table 7.16. WLAN 2.4 GHz Receiver Characteristics on HP RF Chain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sensitivity for 20 MHz Bandwidth [1] [2] [3] | SENS | 802.11b 1 Mbps DSSS [4] | — | -97.5 | — | dBm |
| | | 802.11b 11 Mbps CCK [4] | — | -88 | — | dBm |
| | | 802.11g 6 Mbps OFDM [5] | — | -93 | — | dBm |
| | | 802.11g 54 Mbps OFDM [5] | — | -76.5 | — | dBm |
| | | 802.11n HT20 MCS0 Mixed Mode [6] | — | -92 | — | dBm |
| | | 802.11n HT20 MCS7 Mixed Mode [6] | — | -73 | — | dBm |
| | | 802.11ax HE20 MCS0 SU [7] | — | -91.5 | — | dBm |
| | | 802.11ax HE20 MCS7 SU [7] | — | -72 | — | dBm |
| | | 802.11ax HE20 MCS0 ER [7] | — | -92.5 | — | dBm |
| Maximum Input Level for PER below 10% | $RX_{SAT}$ | 802.11b | — | 3 | — | dBm |
| | | 802.11g | — | -2.5 | — | dBm |
| | | 802.11n | — | -4.5 | — | dBm |
| | | 802.11ax | — | -2.5 | — | dBm |
| RSSI Accuracy Range | $RSSI_{RNG}$ | | — | +/-4 | — | dB |
| Adjacent Channel Interference [8] | ACI | 802.11b 1 Mbps DSSS [4] [9] | — | 43 | — | dB |
| | | 802.11b 11 Mbps CCK [4] [9] | — | 35 | — | dB |
| | | 802.11g 6 Mbps OFDM [5] [10] | — | 38 | — | dB |
| | | 802.11g 54 Mbps OFDM [5] [10] | — | 18 | — | dB |
| | | 802.11n HT20 MCS0 Mixed Mode [6] [10] | — | 32 | — | dB |
| | | 802.11n HT20 MCS7 Mixed Mode [6] [10] | — | 10 | — | dB |
| | | 802.11ax HE20 MCS0 SU [7] [10] | — | 20 | — | dB |
| | | 802.11ax HE20 MCS7 SU [7] [10] | — | 3 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate Adjacent Channel Interference [8] | AACI | 802.11b 1 Mbps DSSS [4 9] | — | 49 | — | dB |
| | | 802.11b 11 Mbps CCK [4 9] | — | 42 | — | dB |
| | | 802.11g 6 Mbps OFDM [5 10] | — | 49 | — | dB |
| | | 802.11g 54 Mbps OFDM [5 10] | — | 27 | — | dB |
| | | 802.11n HT20 MCS0 Mixed Mode [6 10] | — | 48 | — | dB |
| | | 802.11n HT20 MCS7 Mixed Mode [6 10] | — | 26 | — | dB |
| | | 802.11ax HE20 MCS0 SU [7 10] | — | 48 | — | dB |
| | | 802.11ax HE20 MCS7 SU [7 10] | — | 25 | — | dB |

**Note:**

1. RX Sensitivity Variation is up to 2 dB for channels (1, 2, 3, 4, 5, 9, and 10) at typical / room temperature.
2. RX Sensitivity can be degraded up to 3 dB for channels (6, 7, 8, 11, 12, 13 and 14) at typical / room temperature.
3. Sensitivity variation across temperature -40 °C to 85 °C is up to 3 dB
4. 802.11b, Packet size is 1024 bytes, < 8% PER limit, Carrier modulation is non-DCM
5. 802.11g, Packet size is 1024 bytes, < 10% PER limit, Carrier modulation is non-DCM
6. 802.11n, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
7. 802.11ax, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
8. ACI / AACI is calculated as Interferer Power(dBm)- Inband power(dBm)
9. Desired signal power is 6 dB above standard defined sensitivity level
10. Desired signal power is 3 dB above standard defined sensitivity level

### 7.5.3 WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin RF_RX

**Table 7.17. WLAN 2.4 GHz Receiver Characteristics on LP RF Chain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sensitivity for 20 MHz Bandwidth [1] [2] [3] | SENS | 802.11b 1 Mbps DSSS [4] | — | -97 | — | dBm |
| | | 802.11b 11 Mbps CCK [4] | — | -87.5 | — | dBm |
| | | 802.11g 6 Mbps OFDM [5] | — | -92.5 | — | dBm |
| | | 802.11g 36 Mbps OFDM [5] | — | -81.5 | — | dBm |
| | | 802.11n HT20 MCS0 Mixed Mode [6] | — | -91.5 | — | dBm |
| | | 802.11n HT20 MCS4 Mixed Mode [6] | — | -80.5 | — | dBm |
| Maximum Input Level for PER below 10% | $RX_{SAT}$ | 802.11b | — | -8 | — | dBm |
| | | 802.11g | — | -0.5 | — | dBm |
| | | 802.11n | — | -1 | — | dBm |
| RSSI Accuracy Range | $RSSI_{RNG}$ | | — | +/-4 | — | dB |
| Adjacent Channel Interference [7] | ACI | 802.11b 1 Mbps DSSS [4] [8] | — | 43 | — | dB |
| | | 802.11b 11 Mbps CCK [4] [8] | — | 36 | — | dB |
| | | 802.11g 6 Mbps OFDM [5] [9] | — | 38 | — | dB |
| | | 802.11g 36 Mbps OFDM [5] [9] | — | 25 | — | dB |
| | | 802.11n HT20 MCS0 Mixed Mode [6] [9] | — | 32 | — | dB |
| | | 802.11n HT20 MCS4 Mixed Mode [6] [9] | — | 18 | — | dB |
| Alternate Adjacent Channel Interference [7] | AACI | 802.11b 1 Mbps DSSS [4] [8] | — | 46 | — | dB |
| | | 802.11b 11 Mbps CCK [4] [8] | — | 40 | — | dB |
| | | 802.11g 6 Mbps OFDM [5] [9] | — | 43 | — | dB |
| | | 802.11g 36 Mbps OFDM [5] [9] | — | 31 | — | dB |
| | | 802.11n HT20 MCS0 Mixed Mode [6] [9] | — | 43 | — | dB |
| | | 802.11n HT20 MCS4 Mixed Mode [6] [9] | — | 30 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. RX Sensitivity Variation is up to 2 dB for channels (1, 2, 3, 4, 5, 9, and 10) at typical / room temperature
2. RX Sensitivity can be degraded up to 3 dB for channels (6, 7, 8, 11, 12, 13 and 14) at typical / room temperature
3. Sensitivity variation across temperature -40 °C to 85 °C is up to 3 dB
4. 802.11b, Packet size is 1024 bytes, < 8% PER limit, Carrier modulation is non-DCM
5. 802.11g, Packet size is 1024 bytes, < 10% PER limit, Carrier modulation is non-DCM
6. 802.11n, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
7. ACI / AACI is calculated as Interferer Power(dBm)- Inband power(dBm)
8. Desired signal power is 6 dB above standard defined sensitivity level
9. Desired signal power is 3 dB above standard defined sensitivity level

### 7.5.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are refered at IC pin (RF_TX).

**Table 7.18. Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Power [1] [2] | POUT | LE 1 Mbps | — | 19 | — | dBm |
| | | LE 2 Mbps [3] | — | 19 | — | dBm |
| | | LR 500 kbps | — | 19 | — | dBm |
| | | LR 125 kbps [4] | — | 19 | — | dBm |
| Power variation across channels | $POUT_{VAR\_CH}$ | | — | 2 | — | dB |
| Power variation across temperature | $POUT_{VAR\_T}$ | -40 to +85 °C | — | 3 | — | dB |
| Adjacent Channel Power \|M-N\| = 2 | $ACP_{eq2}$ | LE | — | -25 | — | dBm |
| Adjacent Channel Power \|M-N\| > 2 | $ACP_{gt2}$ | LE | — | -31 | — | dBm |
| BLE Modulation Characteristics at 1 Mbps | $MOD_{CHAR}$ | Δf1 Avg | — | 250 | — | kHz |
| | | Δf2 Max | — | 250 | — | kHz |
| | | Δf2 Avg/Δf1 Avg | — | 1.3 | — | |

**Note:**

1. ETSI Max Power should be limited to 10 dBm because device falls under DTS, non-adaptive
2. Refer to the BLE Gain Table section in AN1437 for details on TX power backoff for compliance with regulatory limits.
3. In FCC for data rates 1 Mbps, 2 Mbps, and 500 kbps, Channels in 2476 - 2480 MHz, TX output power will be limited by band edge.
4. In FCC - LR 125 kbps Max Power should be limited to 12 dBm to meet PSD requirement because, device falls under DTS, non-adaptive

### 7.5.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_BLETX).

**Table 7.19. Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Power [1] | POUT | LE 1 Mbps | — | 8 | — | dBm |
| | | LE 2 Mbps [2] | — | 8 | — | dBm |
| | | LR 500 kbps | — | 8 | — | dBm |
| | | LR 125 kbps | — | 8 | — | dBm |
| Power variation across channels | $POUT_{VAR\_CH}$ | | — | 2 | — | dB |
| Power variation across temperature | $POUT_{VAR\_T}$ | -40 to +85 °C | — | 3 | — | dB |
| Adjacent Channel Power \|M-N\| = 2 | $ACP_{eq2}$ | LE | — | -32 | — | dBm |
| Adjacent Channel Power \|M-N\| > 2 | $ACP_{gt2}$ | LE | — | -36 | — | dBm |
| BLE Modulation Characteristics at 1 Mbps | $MOD_{CHAR}$ | Δf1 Avg | — | 248 | — | kHz |
| | | Δf2 Max | — | 249 | — | kHz |
| | | Δf2 Avg/Δf1 Avg | — | 1.3 | — | kHz |

**Note:**

1. Refer to the BLE Gain Table section in AN1437 for details on TX power backoff for compliance with regulatory limits.
2. In FCC, Channel 2480 MHz, 2 Mbps data rate Tx output Power will be limited by Band edge

### 7.5.6 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_BLETX).

**Table 7.20. Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Power | POUT | LE 1 Mbps | — | -0.5 | — | dBm |
| | | LE 2 Mbps | — | -0.5 | — | dBm |
| | | LR 500 kbps | — | -0.5 | — | dBm |
| | | LR 125 kbps | — | -0.5 | — | dBm |
| Power variation across channels | $POUT_{VAR\_CH}$ | | — | 2 | — | dB |
| Power variation across temperature | $POUT_{VAR\_T}$ | -40 to +85 °C | — | 2 | — | dB |
| Adjacent Channel Power \|M-N\| = 2 | $ACP_{eq2}$ | LE | — | -41 | — | dBm |
| Adjacent Channel Power \|M-N\| > 2 | $ACP_{gt2}$ | LE | — | -47 | — | dBm |
| BLE Modulation Characteristics | $MOD_{CHAR}$ | Δf1 Avg | — | 248 | — | kHz |
| | | Δf2 Max | — | 249 | — | kHz |
| | | Δf2 Avg/Δf1 Avg | — | 1.3 | — | kHz |

### 7.5.7 Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: $T_A$ = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

**Table 7.21. Bluetooth Receiver Characteristics for 1 Mbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | $RX_{SAT}$ | Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain | — | 2 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain | — | -2 | — | dBm |
| Sensitivity [1] [2] | SENS | Signal is reference signal, 37 byte payload, BER = 0.1% | — | -96 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017% | — | -94 | — | dBm |
| Signal to co-channel interferer [3] | $C/I_{CC}$ | (see notes)[4] [5] | — | -12 | — | dB |
| N ± 1 Adjacent channel selectivity [3] | $C/I_1$ | Interferer is reference signal at +1 MHz offset[4] [6] [5] [7] | — | -6 | — | dB |
| | | Interferer is reference signal at -1 MHz offset[4] [6] [5] [7] | — | -4 | — | dB |
| N ± 2 Alternate channel selectivity [3] | $C/I_2$ | Interferer is reference signal at +2 MHz offset[4] [6] [5] [7] | — | 19 | — | dB |
| | | Interferer is reference signal at -2 MHz offset[4] [6] [5] [7] | — | 24 | — | dB |
| N ± 3 Alternate channel selectivity [3] | $C/I_3$ | Interferer is reference signal at +3 MHz offset[4] [6] [5] [7] | — | 20 | — | dB |
| | | Interferer is reference signal at -3 MHz offset[4] [6] [5] [7] | — | 31 | — | dB |
| N ≥ \| ± 4\| Alternate channel selectivity [3] | $C/I_4$ | Interferer is reference signal at ≥ \| ± 4\| MHz offset[4] [6] [5] [7] | — | 33 | — | dB |
| Selectivity to image frequency [3] | $C/I_{IM}$ | Interferer is reference signal at image frequency[4] [5] [7] [8] | — | 17 | — | dB |
| Selectivity to image frequency ± 1 MHz [3] | $C/I_{IM\_1}$ | Interferer is reference signal at image frequency +1 MHz[4] [5] [7] [8] | — | 29 | — | dB |
| | | Interferer is reference signal at image frequency -1 MHz[4] [5] [7] [8] | — | 20 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Sensitivities for channels 19, 39 are up to 2 dB lower performance
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB
3. C/I is calculated as Interferer Power(dBm)- Inband power(dBm)
4. 0.1% BER, 37 byte packet size
5. Desired signal = -67 dBm
6. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
7. With allowed exceptions
8. Image frequency is at +4 MHz offset

### 7.5.8 Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: $T_A$ = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

**Table 7.22. Bluetooth Receiver Characteristics for 2 Mbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | $RX_{SAT}$ | Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain | — | 2 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain | — | -6 | — | dBm |
| Sensitivity [1] [2] | SENS | Signal is reference signal, 37 byte payload, BER = 0.1% | — | -93 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017% | — | -91 | — | dBm |
| Signal to co-channel interferer [3] | $C/I_{CC}$ | (see notes)[4] [5] | — | -10 | — | dB |
| N ± 1 Adjacent channel selectivity [3] | $C/I_1$ | Interferer is reference signal at +2 MHz offset[4] [6] [5] [7] | — | 5 | — | dB |
| | | Interferer is reference signal at -2 MHz offset[4] [6] [5] [7] | — | 1 | — | dB |
| N ± 2 Alternate channel selectivity [3] | $C/I_2$ | Interferer is reference signal at +4 MHz offset[4] [6] [5] [7] | — | 14 | — | dB |
| | | Interferer is reference signal at -4 MHz offset[4] [6] [5] [7] | — | 20 | — | dB |
| Selectivity to image frequency [3] | $C/I_{IM}$ | Interferer is reference signal at image frequency[4] [5] [7] [8] | — | 14 | — | dB |
| Selectivity to image frequency ± 2 MHz [3] | $C/I_{IM\_2}$ | Interferer is reference signal at image frequency +2 MHz[4] [5] [7] [8] | — | 24 | — | dB |
| | | Interferer is reference signal at image frequency -2 MHz[4] [5] [7] [8] | — | 5 | — | dB |

**Note:**

1. Sensitivities for channels 19, 39 are up to 2 dB lower performance
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB
3. C/I is calculated as Interferer Power(dBm)- Inband power(dBm)
4. 0.1% BER, 37 byte packet size
5. Desired signal = -67 dBm
6. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
7. With allowed exceptions
8. Image frequency is at +4 MHz offset

### 7.5.9 Bluetooth Receiver Characteristics for 125 kbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: $T_A$ = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

**Table 7.23. Bluetooth Receiver Characteristics for 125 kbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | $RX_{SAT}$ | Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain | — | 3 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain | — | 0 | — | dBm |
| Sensitivity [1] [2] | SENS | Signal is reference signal, 37 byte payload, BER = 0.1% | — | -107 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017% | — | -106 | — | dBm |

**Note:**
1. Sensitivities for channels 19, 39 are up to 2 dB lower performance
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB

### 7.5.10 Bluetooth Receiver Characteristics for 500 kbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: $T_A$ = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

**Table 7.24. Bluetooth Receiver Characteristics for 500 kbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | $RX_{SAT}$ | Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain | — | 3 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain | — | 0 | — | dBm |
| Sensitivity [1] [2] | SENS | Signal is reference signal, 37 byte payload, BER = 0.1% | — | -102.5 | — | dBm |
| | | Signal is reference signal, 255 byte payload, BER = 0.017% | — | -101.5 | — | dBm |

**Note:**
1. Sensitivities for channels 19, 39 are up to 2 dB lower performance
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB

### 7.6 Typical Current Consumption

Figure 7.7 Supply Connection for Current Measurements on page 47 shows the supply connection and measurement point for supply current numbers in this section. A 32.768 kHz crystal is used at pins XTAL_32KHZ_P and XTAL_32KHZ_N.

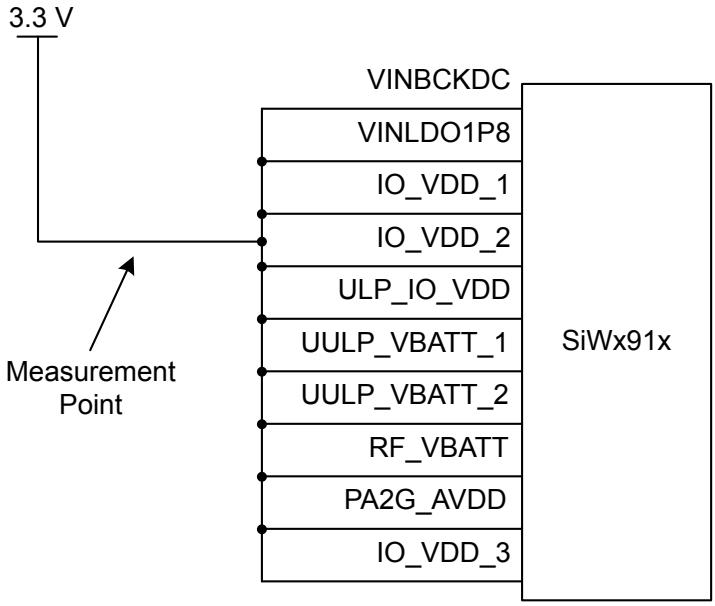


**Figure 7.7. Supply Connection for Current Measurements**

### 7.6.1 WLAN 2.4 GHz 3.3 V Current Consumption

$T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions.

**Table 7.25. WLAN 2.4 GHz 3.3 V Current Consumption**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Listen current | $I_{RX\_LISTEN}$ | LP Chain, 1 Mbps Listen | — | 16.5 | — | mA |
| Active Receive Current | $I_{RX\_ACTIVE}$ | 1 Mbps RX Active, LP Chain | — | 22 | — | mA |
| | | HT20 MCS0, HP Chain | — | 51 | — | mA |
| | | HT20 MCS7, HP Chain | — | 51 | — | mA |
| | | HE20 MCS0, HP Chain | — | 51 | — | mA |
| | | HE20 MCS7, HP Chain | — | 51 | — | mA |
| Transmit Current [1] | $I_{TX}$ | 1 Mbps, HP Chain | — | 240 | — | mA |
| | | HT20 MCS0, HP Chain | — | 230 | — | mA |
| | | HT20 MCS7, HP Chain | — | 180 | — | mA |
| | | HE20 MCS0, HP Chain | — | 220 | — | mA |
| | | HE20 MCS7, HP Chain | — | 170 | — | mA |
| Deep Sleep | $I_{SLEEP}$ | | — | 10 | — | µA |
| Standby Associated, DTIM = 10 | $I_{STBY\_ASSOC}$ | WLAN Keep Alive Every 30 s with 352 KB RAM Retained, Without TCP Keep Alive | — | 65 | — | µA |

**Note:**
1. The absolute maximum device current when transmitting at highest transmit power will not exceed 400 mA.

### 7.6.2 Bluetooth LE Current Consumption

$T_A$ = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions.

**Table 7.26. Bluetooth LE Current Consumption**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| TX Active Current | $I_{TX}$ | LP chain, Tx Power = 0 dBm | — | 10 | — | mA |
| | | LP chain, Tx Power = Max TX power | — | 18 | — | mA |
| RX Active Current | $I_{RX}$ | LP chain | — | 11 | — | mA |
| Advertising, Unconnectable | $I_{ADV\_UC}$ | Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP chain | — | 37 | — | µA |
| Advertising, Connectable | $I_{ADV\_CN}$ | Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP chain | — | 41 | — | µA |
| Connected | $I_{CONN}$ | Connection Interval = 1.28s, No data, Tx Power = 0 dBm, LP chain | — | 36 | — | µA |
| | | Connection Interval = 200 ms, No data, Tx Power = 0 dBm, LP chain | — | 115 | — | µA |

# 8. Reference Schematics, BOM and Layout Guidelines

## 8.1 Schematics

Typical schematic connections are shown in this section. Please refer to following documents for more information.

- Use the provided manufacturing utility for calibrating the external 40 MHz crystal.
- Follow guidelines in Application Note AN1440 for calibrating the power of RF front-end circuitry.
- Follow guidelines in Application Note AN1423 for RF design related aspects.

1. Customers should include provision for calibration at manufacturing.
2. The reference schematics should be followed for optimal RF performance.
3. Use recommended MPNs (Manufacturer Part Number) shown near components wherever possible.

### 8.1.1 System Supplies

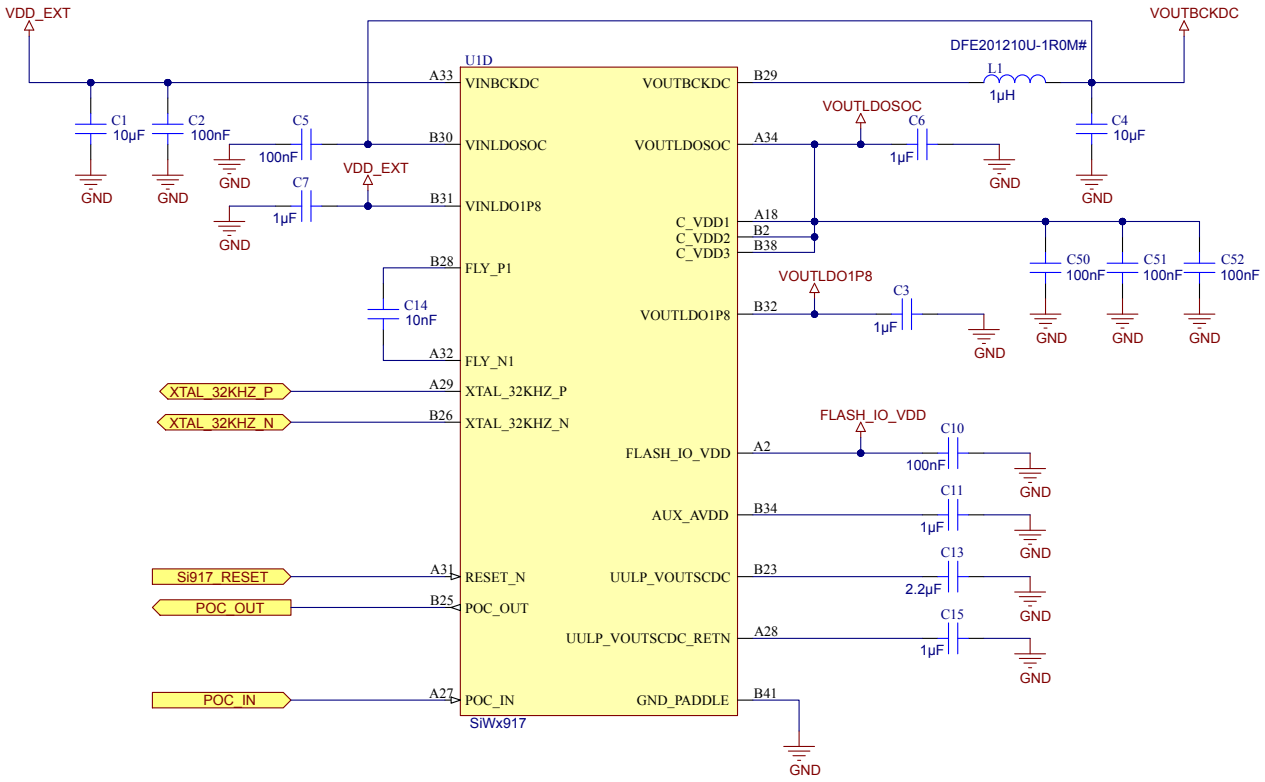


**Figure 8.1. System Power Supplies**

**Note:**

1. Place all the decoupling capacitors close to the IC pins.
2. It is recommended to follow star routing for the supply pins from main supply source and add test points to all supply pins.
3. VDD_EXT supply voltage must match the recommended operating conditions of power supply pins.

### 8.1.2 RF Supplies

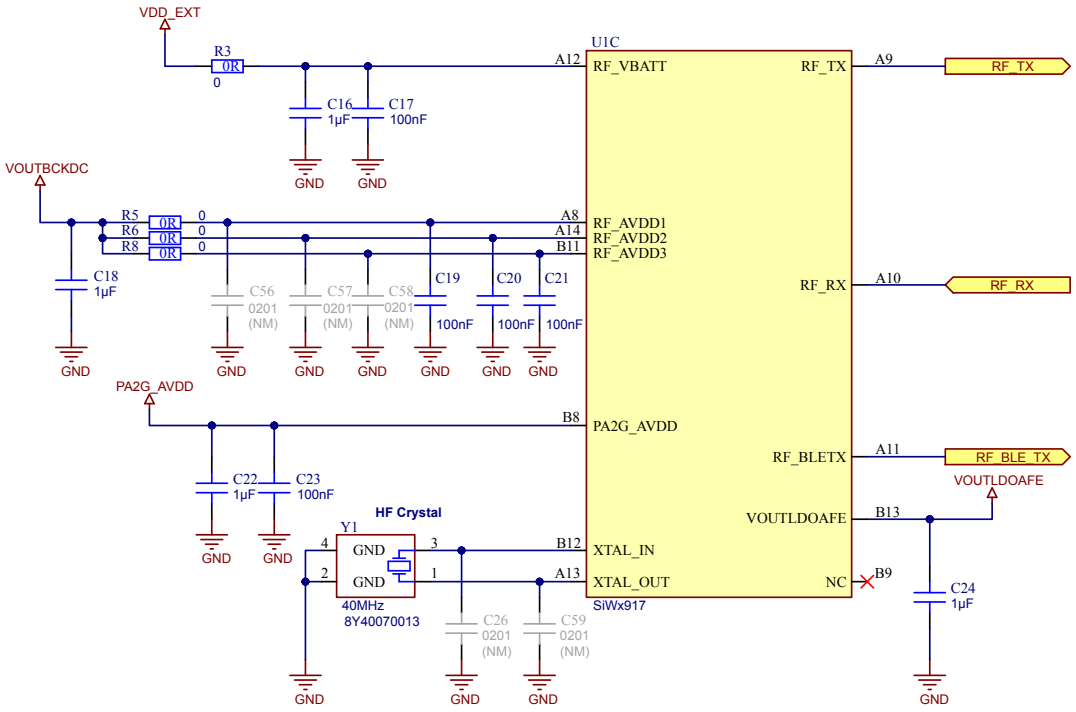


**Figure 8.2. RF Power and HF Crystal Support**

**Note:**

1. Do not share routing between PA2G_AVDD and RF_VBATT. Use star routing for PA2G_AVDD and RF_VBATT.
2. VOUTBCKDC should be star routed to RF_AVDD supply pins.
3. VDD_EXT supply voltage must match the recommended operating conditions of power supply pins.
4. Use recommended part for high frequency crystal 40 MHz. This 40 MHz crystal can be tuned with the internal capacitors in the device.
5. PA2G_AVDD can be independent of other supplies and it must be operated at 3.3V only.
6. C26 and C59 are optional tuning capacitors.
7. R5, C56, R6, C57, R8 and C58 are placeholder components for power supply noise filtering.
8. R3 is a placeholder component for power supply noise filtering.
9. It is recommended to add test points to all supply pins.

### 8.1.3 GPIO Supplies

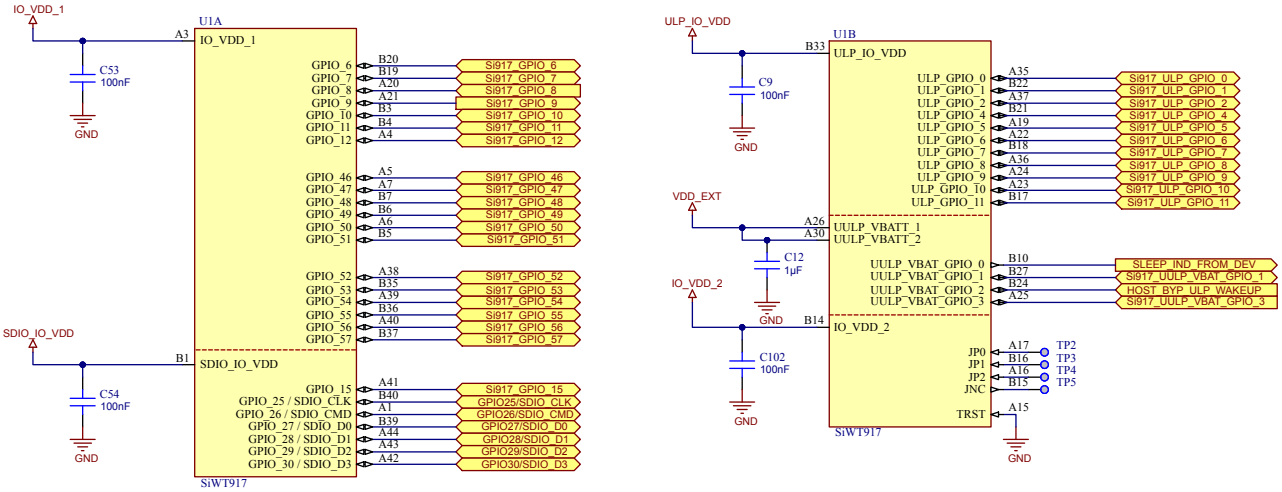


**Figure 8.3. GPIO Supply Domains**

**Note:**

1. IO_VDD_1, IO_VDD_2, IO_VDD_3, ULP_IO_VDD can be powered independently by different Voltage Sources based on their corresponding signals voltage levels requirements. Voltages must be as per the recommended Operating conditions
2. Place C12 close to UULP_VBATT_2 pin.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.
4. VDD_EXT supply voltage must match the recommended operating conditions of power supply pins.
5. It is recommended to add test points to all supply pins.

### 8.1.4 RF Frontend

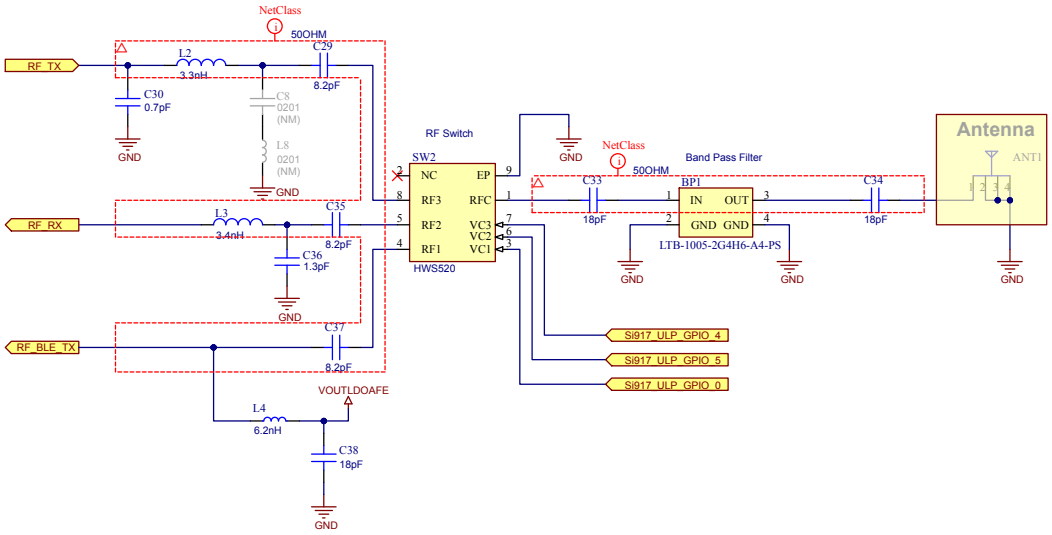


**Figure 8.4. Option 1: RF Frontend with External Switch**

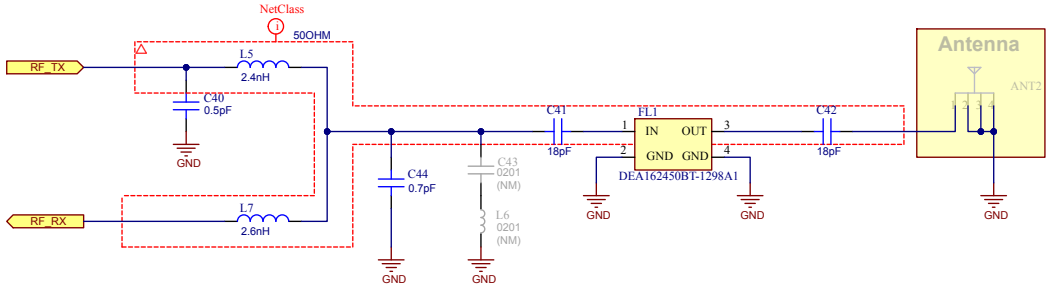


**Figure 8.5. Option 2: RF Frontend with Internal Switch**

**Note:**

1. ANT1 and ANT2: In-built antenna or an external antenna (with U.FL connector) can be used.
2. The 8 dBm BLE LP transmit path on RF_BLETX is not available for the internal switch option.
3. Maintain 50 ohm characteristic impedance for RF traces.
4. It is recommended to add microwave coaxial switch connector (Example : Murata's MM8430-2610RA1) or U.FL connector for conducted measurements.
5. Additional matching circuit to be provided near the antenna, based on antenna used and location on the board.
6. For the external RF switch option, follow the reference layout for RF front-end circuit from IC pins up to at least RF switch.
   - Provision C38 on the VOUTLDOAFE trace. C38 must be placed close to L4.
   - Trace routing from the VOUTLDOAFE pin to inductor L4 must be short, with a maximum length of 15 mm.
   - If the trace length is between 7.5 mm and 15 mm, mount capacitor C38.
7. For the internal RF switch option, follow the reference layout for RF front-end circuit from IC pins up to at least the FL1 band pass filter.
8. C8 and L8 (external switch) or C43 and L6 (internal switch) are placeholder components for harmonic emission filtering.
9. Follow guidelines in Application Note AN1440 for calibrating the power of RF front-end circuitry.
10. Follow guidelines in Application Note AN1423 for RF design related aspects.
11. There will be significant RF performance degradation if antenna select signals (ULP_GPIO_4, ULP_GPIO_5,ULP_GPIO_0) are powered at 1.8 V from the ULP_IO_VDD supply. It is recommended to supply ULP_IO_VDD from the 3.3 V supply.
12. There will be slight RF performance degradation with the internal RF switch option. Refer to Application Note AN1423 for details.

13. ULP_GPIO_0/4/5 are used to control the switch in external switch configuration. These signals map to the following functions:
    - ULP_GPIO_0: RF_BLETX pin active
    - ULP_GPIO_4: RF_TX pin active
    - ULP_GPIO_5: RF_RX pin active

### 8.1.5 LF Clock Options

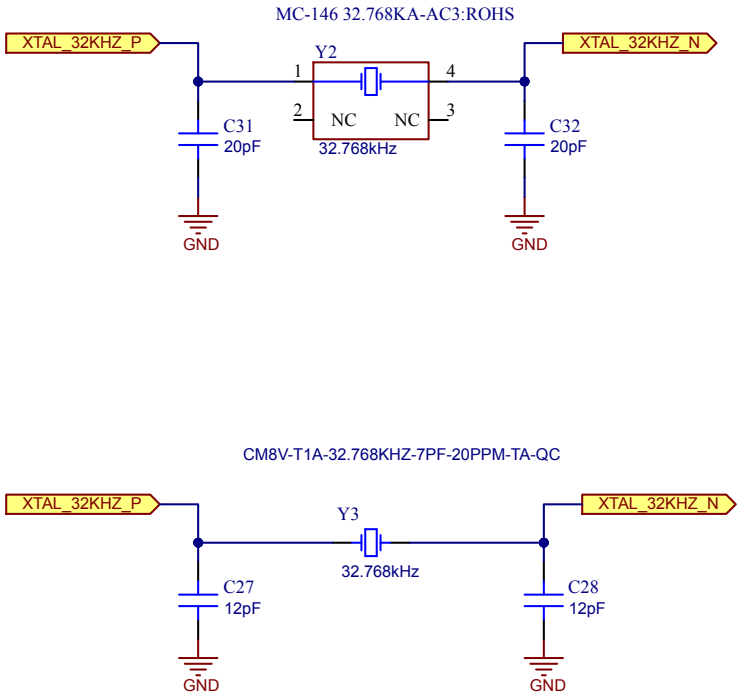


**Figure 8.6. 32.768 kHz Clock Options**

**Note:**

1. Two different crystals and their circuits are shown in the figure. Use one of them only.
2. Load capacitors for external crystals must be fine-tuned based on the layout design.

### 8.1.6 Reset

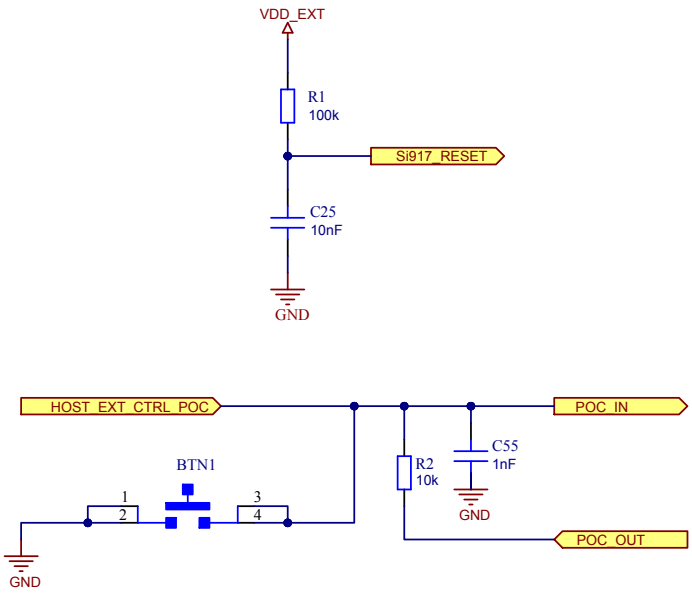


**Figure 8.7. Reset Configuration**

**Note:**

1. The configuration shown allows for blackout monitor functionality along with external reset of the SiWx917 IC.
2. The POC_IN signal connects to the POC_IN pin on the SiWx917. POC_IN resets all the internal blocks of the IC.
3. The Si917_RESET signal connects to the RESET_N pin on the SiWx917. It is recommended to use the RC filter as shown. RESET_N is an open-drain output pin that will be pulled low when POC_IN goes low.
4. The POC_OUT signal connects to the POC_OUT pin on the SiWx917. POC_OUT is an active-low, push-pull output from the internal blackout monitor. In this configuration, it is isolated from the external HOST_EXT_CTRL_POC signal with a series resistor. In applications without external host control (HOST_EXT_CTRL_POC), POC_OUT may be directly connected to POC_IN. Without external host control to the POC_IN pin, the IC cannot be reset multiple times after power-on.
5. The HOST_EXT_CTRL_POC signal connects to a GPIO of an external host processor. In this configuration, HOST_EXT_CTRL_POC must be an open-drain output to allow POC_OUT to control POC_IN.
6. VDD_EXT must be at the same voltage level as the UULP_VBATT_2 supply pin.
7. HOST_EXT_CTRL_POC must be at the same voltage level as the UULP_VBATT_1 supply pin.

### 8.1.7 Host Interface

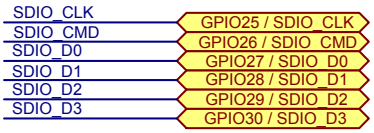


**Figure 8.8. Host Interface Options**

**Note:**

1. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification version 2.0.

### 8.2 BOM

Manufacturer part numbers provided in this section are a guideline, and may be replaced with suitably equivalent components as needed. Device characteristics and performance are measured using the specified crystals, supply filtering, and RF frontend circuitry.

**Table 8.1. SiWT917 Circuitry: Mandatory Components (Power Mangement + Crystal + SiWT917 IC)**

| S.No. | Quantity | Designator | Value | Manufacturer | Manufacturer PN | Description |
|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 10 µF | Murata | GRM188R61C106MAALD | CAP CER 0603 X5R 10uF 16V 20% |
| 2 | 10 | C2, C5, C9, C10, C50, C51, C52, C53, C54, C102 | 100 nF | Murata | GRT155R71H104KE01D | CAP CER 0402 X7R 0.1uF 50V 10% |
| 3 | 10 | C3, C6, C7, C11, C12, C15, C16, C18, C22, C24 | 1 µF | Murata | GRM033R61C105ME15D | CAP CER 0201 X5R 1uF 16V 20% |
| 4 | 1 | C4 | 10 µF | CalChip | GMC21X7R106K25NT | CAP CER 0805 X7R 10uF 25V 10% |
| 5 | 1 | C13 | 2.2 µF | Murata | GRM033R61A225ME47D | CAP CER 0201 X5R 2.2uF 10V 20% |
| 6 | 1 | C14 | 10 nF | Murata | GRM033R61C103KA12D | CAP CER 0201 X5R 10nF 16V 10% |
| 7 | 5 | C17, C19, C20, C21, C23 | 100 nF | Murata | GRM033R61C104KE14J | CAP CER 0201 X5R 100nF 16V 10% |
| 8 | 1 | L1 | 1 µH | Murata | DFE201210U-1R0M=P2 | IND Fixed 0805 1uH 2A 95mOhm 20% |
| 9 | 4 | R3, R5, R6, R8 | 0 Ω | Yageo | RC0201FR-07200RL | RES 0201 0R |
| 10 | 1 | U1 | SiWT917 | Silicon Labs | SiWT917 | Choose the suitable OPN from List of OPNs from Ordering Information section in datasheet. |
| 11 | 1 | Y1 | 40 MHz | TXC | 8Y40070013 | CRYSTAL 2.0X1.6mm 40MHz 8pF 8ppm |

**Table 8.2. SiWT917: RF Front-End Options (one of them has to be used mandatorily)**

| S. No. | Quantity | Designator | Value | Manufacturer | Manufacturer PN | Description |
|---|---|---|---|---|---|---|
| **Option 1: RF Matching +External RF Switch + Band Pass Filter** | | | | | | |
| 12 | 1 | ANT1 | 2.45 GHz | Johanson | 2450AT18D0100001 | ANT SMD 3.2X1.6X1.2MM 2.4GHz |
| 13 | 1 | BP1 | 2.45 GHz | Maglayers | LTB-1005-2G4H6-A4-PS | FILTER BAND PASS 0402-4Pin 2.45GHz 100MHz |
| 14 | 3 | C29, C35, C37 | 8.2 pF | Murata | GJM0335C1E8R2BB01 | CAP CER 0201 C0G 8.2pF 25V ±0.1pF |

| S. No. | Quantity | Designator | Value | Manufacturer | Manufacturer PN | Description |
|---|---|---|---|---|---|---|
| 15 | 1 | C30 | 0.7 pF | Murata | GJM0335C1HR70WB01 | CAP CER 0201 C0G 0.7pF 50V ±0.05pF |
| 16 | 2 | C33, C34, C38 | 18 pF | Murata | GRM0335C1H180GA01 | CAP CER 0201 C0G 18pF 50V 2% |
| 17 | 1 | C36 | 1.3 pF | Murata | GJM0335C1E1R3WA01D | CAP CER 0201 C0G 1.3pF 50V ±0.05pF |
| 18 | 1 | L2 | 3.3 nH | Murata | LQP03HQ3N3B02 | IND Fixed 0201 3.3nH 500mA 170mOhm ±0.1nH |
| 19 | 1 | L3 | 3.4 nH | Murata | LQP03TN3N4C02 | IND Fixed 0201 3.4nH 450mA 250mOhm ±0.2nH |
| 20 | 1 | L4 | 6.2 nH | Murata | LQP03HQ6N2H02 | IND Fixed 0201 6.2nH 400mA 250mOhm 3% |
| 21 | 1 | SW2 | HWS520 | Hexawave | HWS520 | IC RF SWITCH SP3T 6GHz USON8L |
| **Option 2: Internal RF Switch + Matching + BPF** | | | | | | |
| 22 | 1 | ANT2 | 2.4 GHz | Johanson | 2450AT18D0100001 | ANT SMD 3.2X1.6X1.2MM 2.4GHz |
| 23 | 2 | C41, C42 | 18 pF | Murata | GJM0335C1E180GB01D | CAP CER 0201 C0G 18pF 25V 2% |
| 24 | 1 | C40 | 0.5 pF | Murata | GJM0335C1ER50WB01 | CAP CER 0201 C0G 0.5pF 25V ±0.05pF |
| 25 | 1 | C44 | 0.7 pF | Murata | GJM0335C1ER70WB01 | CAP CER 0201 C0G 0.7pF 25V ±0.05pF |
| 26 | 1 | FL1 | 2.45 GHz | TDK | DEA162450BT-1298A1 | FILTER BAND PASS 1608 2400MHz 2500MHz |
| 27 | 1 | L5 | 2.4 nH | Murata | LQP03TN2N4B02 | IND Fixed 0201 2.4nH 500mA 200mOhm ±0.1nH |
| 28 | 1 | L7 | 2.6 nH | Murata | LQP03TN2N6B02 | IND Fixed 0201 2.6nH 500mA 200mOhm ±0.1nH |

**Table 8.3. SiWT917: External 32.768 kHz Clock Options**

| S. No. | Quantity | Designator | Value | Manufacturer | Manufacturer PN | Description |
|---|---|---|---|---|---|---|
| **Option 1a: 32.768 kHz Crystal** | | | | | | |
| 29 | 1 | Y2 | 32.768 kHz | Epson | MC-146 32.768KA-AC3:ROHS | CRYSTAL 7.0x1.5mm 32.768kHz 9pF 20ppm |
| 30 | 2 | C31, C32 | 20 pF | Murata | GRM0335C1H200GA01 | CAP CER 0201 C0G 20pF 50V 2% |
| **Option 1b: 32.768 kHz Crystal** | | | | | | |
| 31 | 2 | C27, C28 | 9 pF | Murata | GJM0335C1E9R0WB01 | CAP CER 0201 C0G 9pF 25V ±0.05pF |
| 32 | 1 | Y3 | 32.768 kHz | Micro Crystal | CM8V-T1A-32.768KHZ-7PF-20PPM-TA-QC | CRYSTAL 2.0x1.2mm 32.768kHz 7pF 20ppm |

**Table 8.4. SiWT917: Discrete Parts (BTN1 part is optional and need not be used for every use-case)**

| S. No. | Quanti-ty | Designator | Value | Manufacturer | Manufacturer PN | Description |
|---|---|---|---|---|---|---|
| 33 | 1 | BTN1 | PTS810 SJM 250 SMTR LFS | C&K | PTS810 SJM 250 SMTR LFS | Tactile Switch SPST-NO 0.05A 16V |
| 34 | 1 | R1 | 100 kΩ | Yageo | RC0201FR-07100KL | RES 0201 100K 1/20W 1% 200ppm |
| 35 | 1 | C25 | 10 nF | Murata | GRM033R61C103KA12D | CAP CER 0201 X5R 10nF 16V 10% |
| 36 | 1 | R2 | 10 kΩ | Yageo | RC0201FR-0710KL | RES 0201 10K 1/20W 1% 200ppm |
| 37 | 1 | C55 | 1 nF | Murata | GRM033R71C102KA01D | CAP CER 0201 X7R 1nF 16V 10% |

### 8.3 Layout Guidelines for DR-QFN

The following guidelines outline the integration of the DR-QFN:

1. The following supply pins must be star routed from the supply source:
   a. VINBCKDC
   b. VINLDO1P8
   c. IO_VDD_1, IO_VDD_2, IO_VDD_3
   d. ULP_IO_VDD
   e. UULP_VBATT_1
   f. UULP_VBATT_2
   g. RF_VBATT
   h. PA2G_AVDD
2. The RF traces must have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
3. Each GND pin must have a separate GND via.
4. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
5. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
6. Add GND copper pour underneath IC in all layers, for better thermal dissipation.
7. Provision an RF shield around the IC and RF circuitry, excluding antenna portion.
8. Refer to RF Matching and Layout Design Guide Application Note AN1423 for more details about following RF related design aspects.
9. Add 5 x 5 thermal vias (25 total) of at least 10-mils drill size equally placed on the "GND paddle" for better thermal dissipation.
10. The layout guidelines for the buck DC-DC are as follows:

    Minimize the loop area formed by inductor switching node, output capacitors & input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance & resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components.
    a. The capacitor for VINBCKDC (C1) should be very close to the IC pin and the ground pad of the capacitor should have direct vias to the ground plane.
    b. The inductor (L1) should be close to IC pin VOUTBCKDC and the buck capacitor (C4) should be placed close to the inductor. The ground pad of the capacitor should have direct vias to the ground plane underneath.
    c. The ground plane underneath the buck inductor (L1) in the top layer should be made as an isolated copper patch and should descend down to the main ground layer through multiple vias.
    d. The path from VOUTBCKDC to VINLDOSOC is a high current path. The trace should be as short and wide as possible and it is recommended to run grounded shield traces on either side of this high current trace.
    e. The capacitor on VINLDOSOC (C4) should be very close to the IC pin & the ground pad of the capacitor should have direct vias to the ground plane underneath.
11. Refer to Silicon Labs' radio board designs and Application Note AN1423 for layout examples.

### 8.4 Calibration Requirements

The IC design circuit, as shown in Section 8.1 Schematics, involves discrete components in the RF path and 50-ohm PCB traces. There can be variations in manufacturing tolerances from these discrete components and part-to-part IC variation leading to board-to-board performance variation in power level.

Accurate control over TX power is required for regulatory purposes. It is recommended that one performs TX Gain offset calibration on the end-product to compensate for these board-to-board power variations. This requires provision for conducted power measurement on end-product. If the customer does not have the capability for conducted power measurement and this calibration, then fixed TX power back off may be required to ensure regulatory compliance.

Refer to Application Note AN1440 for calibrating the power of RF front-end circuitry, and the manufacturing utility software for calibration of crystal frequency.

# 9. Package Specifications

## 9.1 Package Outline

**Table 9.1. Package Dimensions - DR-QFN**

| Parameter | Value (LxWxH) | Units |
|---|---|---|
| Package Dimensions | 7 x 7 x 0.85 | mm |
| Tolerance | ±0.1 | mm |

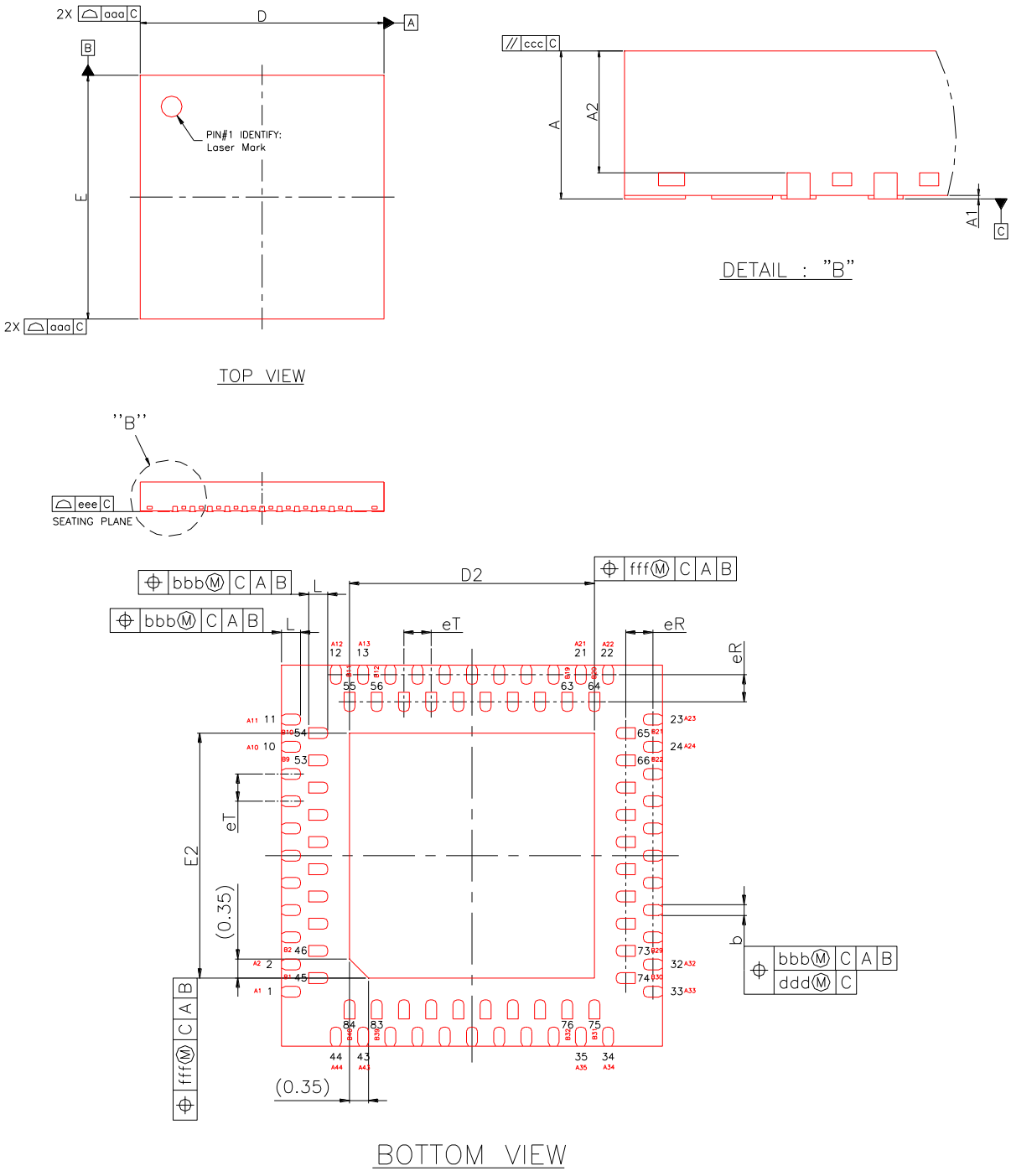


**Figure 9.1. Package Outline - DR-QFN**

**Table 9.2. PCB Landing Pattern - DR-QFN**

| Dimension | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.75 | 0.85 | 0.95 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | 0.65 | 0.70 | 0.75 |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 4.40 | 4.50 | 4.60 |
| E2 | 4.40 | 4.50 | 4.60 |
| eT | 0.50 BSC | | |
| eR | 0.50 BSC | | |
| L | 0.30 | 0.35 | 0.40 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.20 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 9.2 PCB Land Pattern

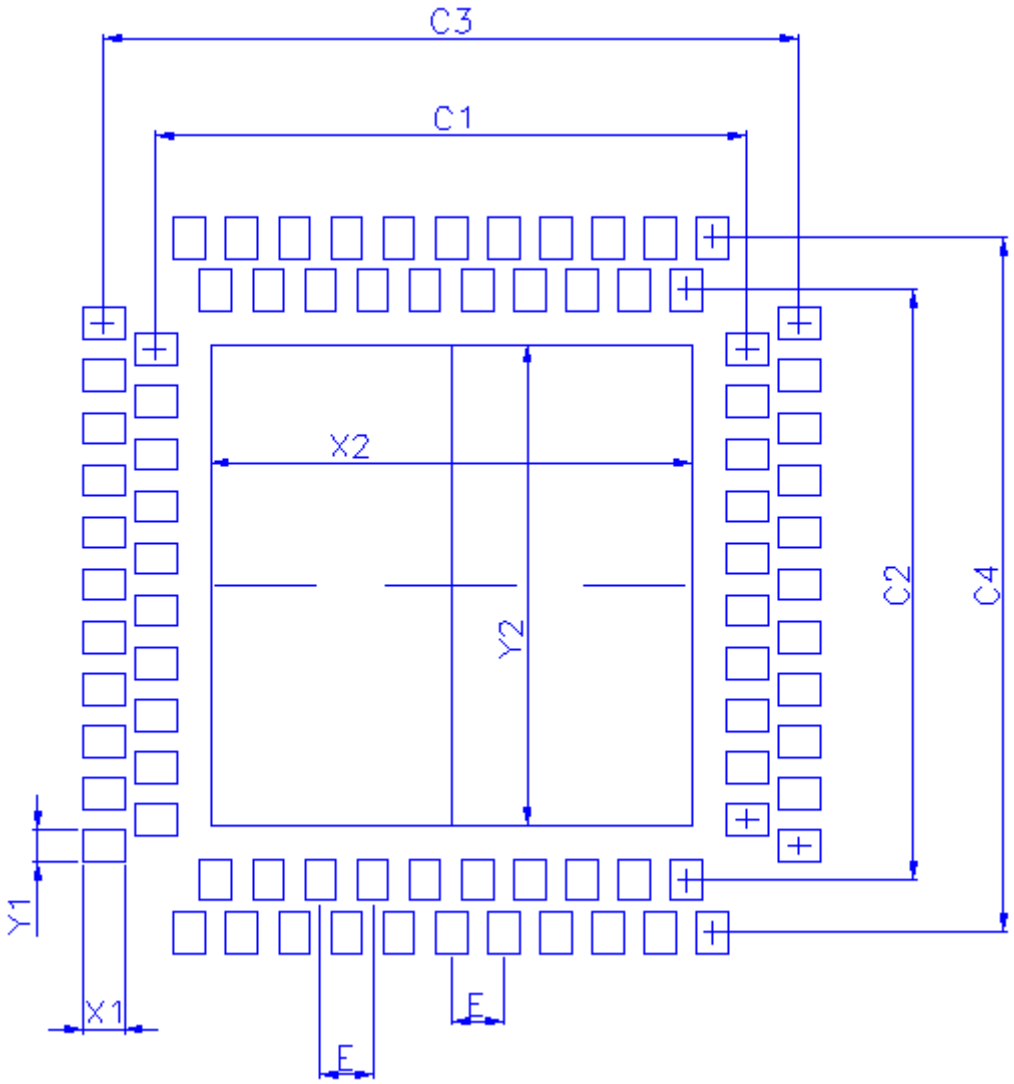


**Figure 9.2. PCB Landing Pattern - DR-QFN**

**Table 9.3. Dimension Table**

| Dimension | mm |
|---|---|
| C1 | 5.65 |
| C2 | 5.65 |
| C3 | 6.65 |
| C4 | 6.65 |
| E | 0.5 BSC |
| X1 | 0.40 |
| X2 | 4.60 |
| Y1 | 0.25 |
| Y2 | 4.60 |

**Note:**

**General**

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

**Solder Mask Design**

1. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 10 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.100 mm (4 mils).
3. The stencil aperture to land pad size recommendation is 80% paste coverage.

*Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

### 9.3 Top Marking

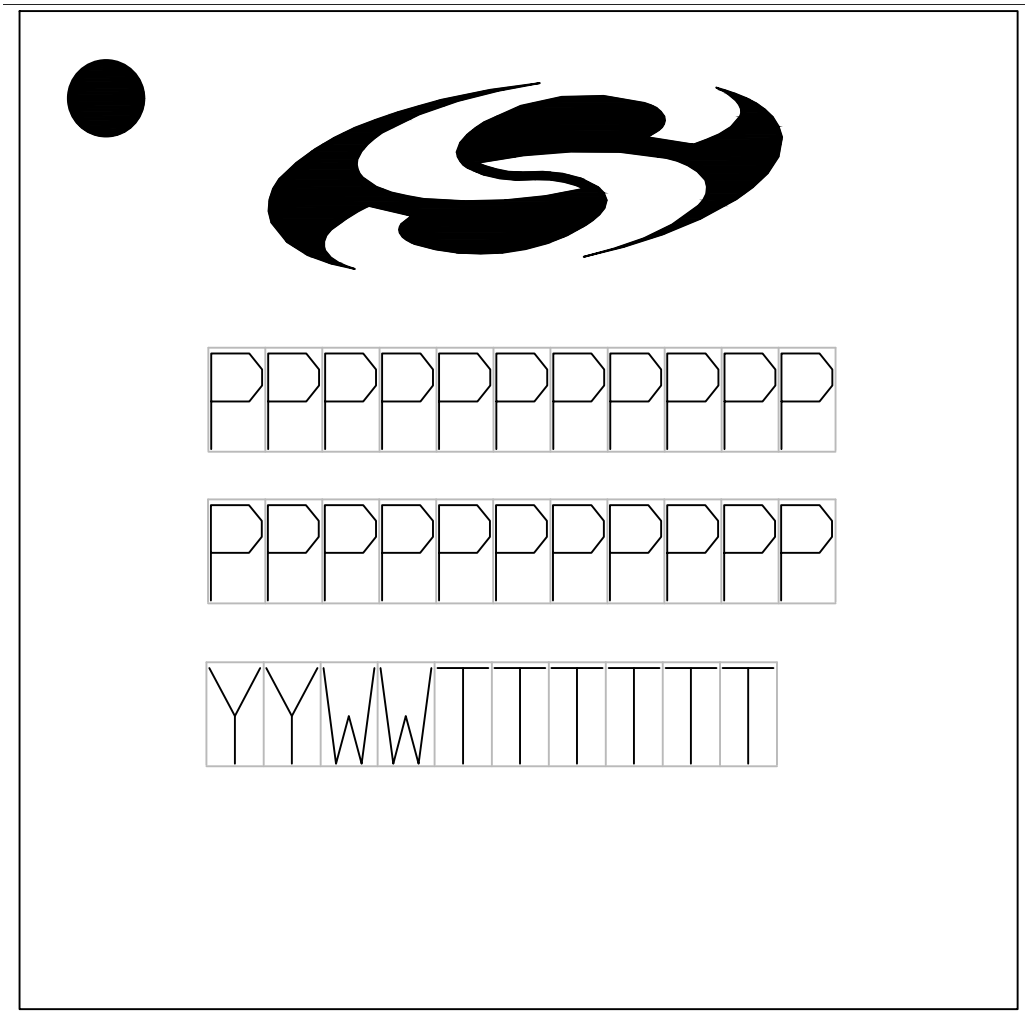


**Figure 9.3. Top Marking**

**Mark Description**

The package marking consists of:

- PPPPPPPPPP - Part number designation in both the rows
- YYWWTTTTTT
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - TTTTTT – A trace or manufacturing code. The first letter is the device revision.

# 10. SiWT917 Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using SiWT917. These documents will be available on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

### Resource Location

SiWT917 Document Library: https://docs.silabs.com/wifi91xrcp/2.10.1/wifi91xrcp-developing-in-rcp-mode/

Technical Support: http://www.silabs.com/support/

# 11. Revision History

**Revision 1.0**

December, 2024

- Removed LVCMOS external 32.768 kHz clock option. A 32.768 kHz crystal is mandatory for all applications requiring low-power Wi-Fi, BLE, and Coex sleep.
- 6.1 Pin Diagram: Corrected name of UULP_VOUTSCDC pin
- 7. Electrical Specifications:
  - 7.1 Absolute Maximum Ratings: Added absolute maximum voltage and current ratings for I/O pins
  - 7.3.2 Power On Control (POC) and Reset Clarified POC and Reset functionality
  - Removed specification table for internal RC boot oscillator and clarified this is only for boot-up
  - 7.5 RF Characteristics  Added supported WLAN channels for different regions
  - All electrical specifications updated with final char results and test limits
- 8. Reference Schematics, BOM and Layout Guidelines
  - Updated schematic images with text-searchable versions
  - Corrected manufacturer part details for C36, L2, L3, C41, C42, C40, C44, L5, and L7
  - Added notes for position and usage of capacitor C38

**Revision 0.5**

August, 2024

Initial version.

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