

# 200602785 Errata Revision 0.5 for EFR32MG21 and Errata Revision 0.4 for EFR32BG21

Bulletin Issue Date: 6/2/2020

Effective Date: 6/2/2020

# **Description of Change**

Silicon Labs announces Errata revision 0.5 for EFR32MG21 and Errata revision 0.4 for EFR32BG21 Wireless SoCs. The following errata and workarounds have been added. TIMER\_E301 — Continuous Overflow and Underflow Interrupts in Quadrature Counting Mode USART\_E301 — Possible Data Transmission on Wrong Edge in Synchronous Mode USART\_E302 — Additional SCLK Pulses are generated in the USART Synchronous Mode

USART\_E302 — Additional SCLK Pulses are generated in the USART Synchronous USART\_E303 — USART DMA Transactions Fail with Slow Peripheral Clocks

WDOG\_E301 – Clear Command is Lost Upon EM2 Entry

See the Revision History of the errata documents for a complete list of changes.

## **Reason for Change**

Errata document updated for new errata items and workarounds.

## **Product Identification**

Existing Part # EFR32BG21A010F1024IM32-B EFR32BG21A010F1024IM32-BR EFR32BG21A010F512IM32-B EFR32BG21A010F512IM32-BR EFR32BG21A010F768IM32-B EFR32BG21A010F768IM32-BR EFR32BG21A020F1024IM32-B EFR32BG21A020F1024IM32-BR EFR32BG21A020F512IM32-B EFR32BG21A020F512IM32-BR EFR32BG21A020F768IM32-B EFR32BG21A020F768IM32-BR EFR32MG21A010F1024IM32-B EFR32MG21A010F1024IM32-BR EFR32MG21A010F512IM32-B EFR32MG21A010F512IM32-BR EFR32MG21A010F768IM32-B EFR32MG21A010F768IM32-BR EFR32MG21A020F1024IM32-B EFR32MG21A020F1024IM32-BR EFR32MG21A020F512IM32-B EFR32MG21A020F512IM32-BR EFR32MG21A020F768IM32-B EFR32MG21A020F768IM32-BR EFR32BG21A010MXXXXIM32-B EFR32BG21A010M1XXXXM32-BR EFR32MG21A010MXXXXIM32-B EFR32MG21A010MXXXXIM32-BR EFR32MG21A020MXXXXIM32-B EFR32MG21A020MXXXXIM32-BR This change is considered a minor change which does not affect form, fit, function, quality, or reliability. The information is being provided as a customer courtesy.

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Silicon Laboratories Inc. 400 West Cesar Chavez Austin, TX 78701

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