LPWAN SERIES

Presentation Will Begin Shortly

tech talks UPCOMING SESSIONS

FEB 16TH	Amazon Sidewalk: Using Battery-Powered Sensors
MAR 16TH	Getting Started with Amazon Sidewalk
APR 13TH	Introducing FG25 for Wi-SUN FAN 1.1
MAY 11TH	Optimizing FG23 for Battery Life & Performance
JUN 8TH	Designing Long Range Devices with Amazon Sidewalk

We will begin in: 0:00

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2023 tech talks
WEBINAR SERIES

Welcome

Optimizing FG23 for Battery Life and Performance

Chad Steider
Zoltan Than
Philipp Luebeck

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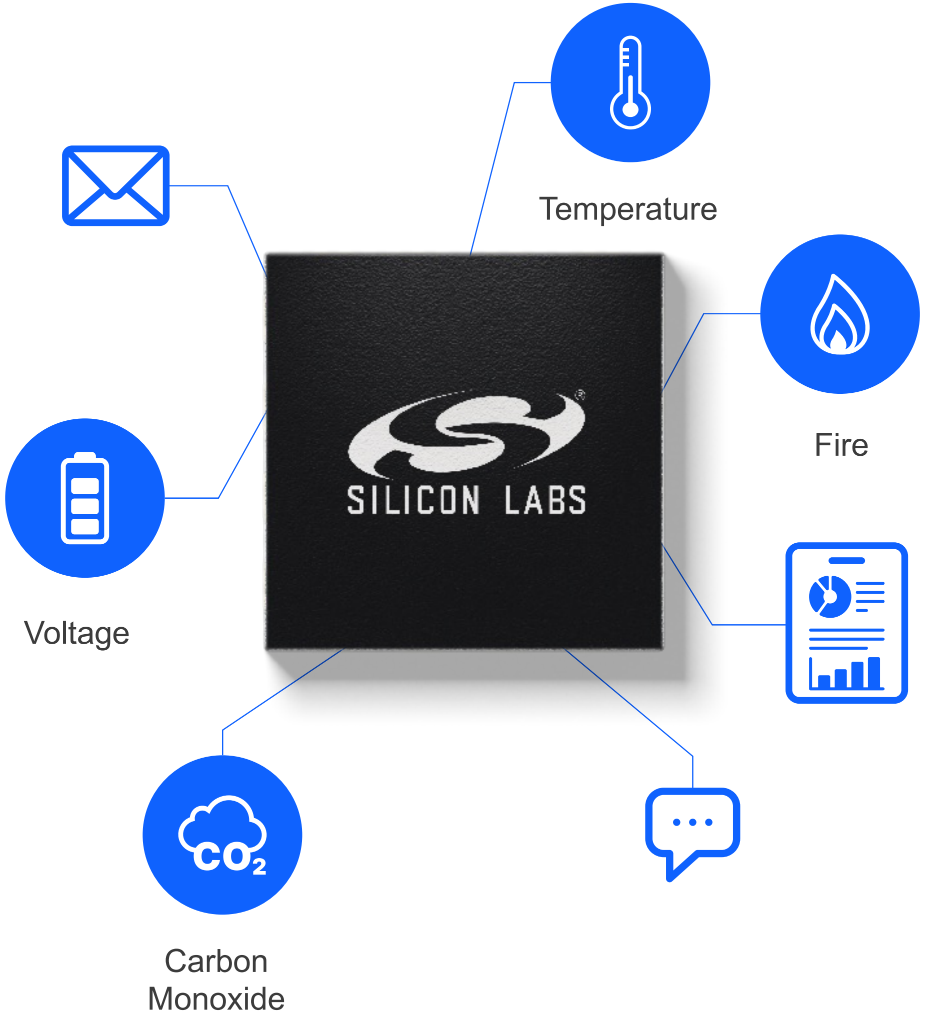
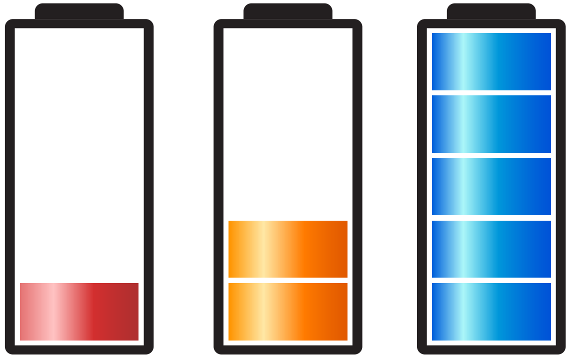
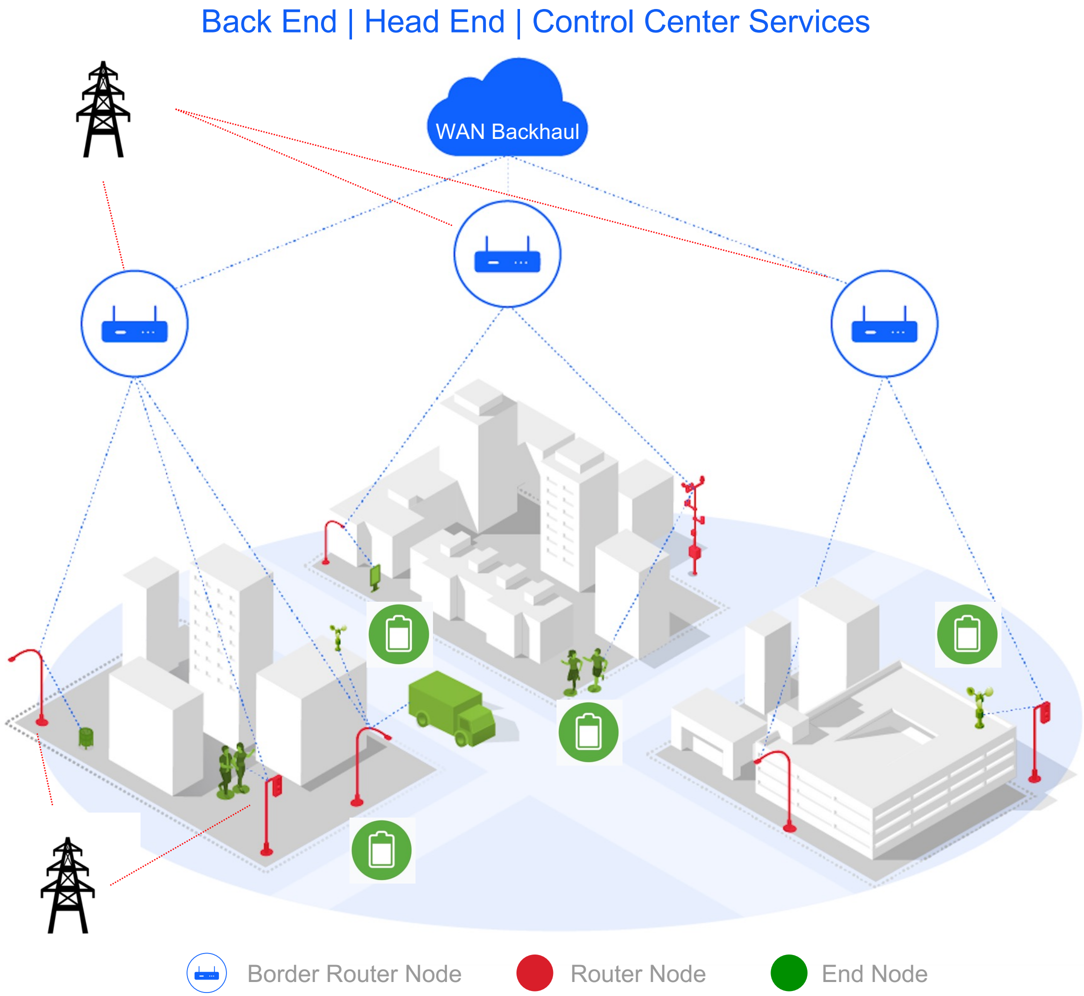
Why Battery Operated?





- Resource sustainability
- Consumer awareness
- Cost impacts
- User convenience
- Regulatory environment
- Functionality additions

Architecture and types of devices



- **Similarities vs. differences in IoT networks**
- **Mix of line-powered and battery-operated nodes**
  - Gateway/Border router
    - Line Powered
  - Routing nodes
    - Line powered or battery operated
  - End nodes
    - Battery operated

Use Cases Drive Battery Requirements

- **Regular vs. User-triggered**
  - Device behavior and connection interval determined by the needs of the network
  - Determination of regular vs triggered reporting strategy can greatly impact power consumption of devices
- **Wireless technology choice affects battery lifetime**
  - Different network selections have different requirements for advertising interval, connection maintenance, and protocol overhead that can greatly affect power consumption

Wi SUN
Proprietary
zigbee
sigfox
Long Range PHY (Proprietary)
Connect

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End-device challenges and solutions

- Environment sensing functionality
- MCU wake-up periods affect consumption
- MCU activity minimisation required for sensing
- LESENSE and PRS major contributors for minimising sensing time

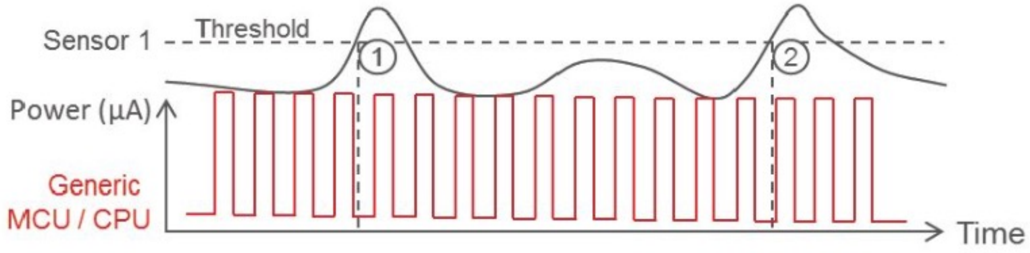

Figure 1: High Energy Consumption with CPU Polling and Active during Every Measurement

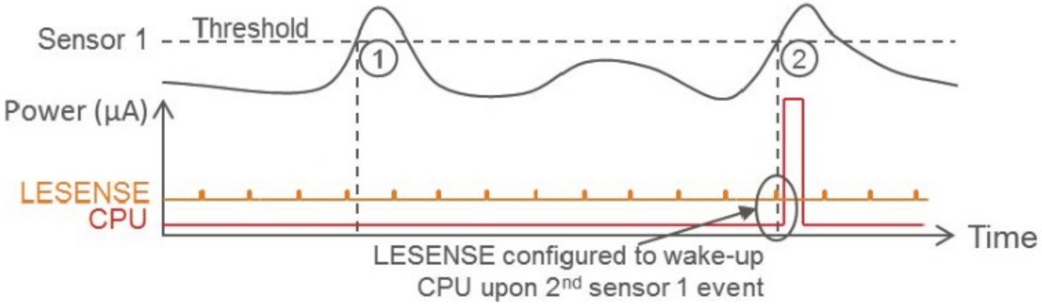

Figure 2: Each LESENSE-Enabled Sensor Input/Output is Independent and Configurable

FG23 and FGM230S for battery operated sub-GHz devices

The first sub-GHz SoCs to combine long-range RF & energy efficiency with PSA™ Level 3 security

- **Simultaneous 1+ mile wireless connectivity & 10+ year battery operation**
- **Secure Vault™ (certified PSA Level 3) safeguards against hardware and software attacks**
- **Broad support for sub-GHz frequencies, modulations and wireless protocols**
- **868 MHz and 915 MHz sub-GHz frequencies, modulations and wireless protocols**
- **Compact form factor and antenna matching with SiP module package**

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Analog Peripheral Focused Techniques

Minimize Analog Energy Use Through Fine-Tuning

- **Suspend the IADC clock when using PRS triggering**
  - Doesn't matter if the PRS producer is a timer (e.g. LETIMER) or GPIO
  - Current draw reduction is appreciable (5.5x for single-channel sampling at 100 Hz, better still for asynchronous use cases)

- **Use the duty-cycled sample-and-hold ACMP inputs in EM2/3 low-energy modes**
  - Available for the reference options (1.25V, 2.5V, and divided AVDD) and the VSENSE0/1 power supply monitoring channels (AVDD, DVDD, and VDDIO)
  - Per comparator savings of 4 µA for reference inputs and 1.8 µA for supply monitor inputs

- **Minimize VDAC drive time with sample-off mode in EM2/3 low-energy modes**
  - Take advantage of the RC filtering probably already connected to the VDAC main output(s)
  - Use sample-off mode to drive the VDAC outputs at less than 100% duty cycle
  - At 30% duty cycle, for example, current reduction is 50% whether just one or both VDAC outputs are driven

Turn to Hardware Functionality to Save Energy

- **Stop reading the battery voltage with the IADC**
  - Hard to get accurate results when load currents cause the battery output voltage to fluctuate
  - Use the ACMP VSENSE0 channel to monitor AVDD in EM2 instead when quiescent current is low
  - Set an initial trip voltage to request an interrupt to warn about the low battery condition
  - Go into EM4 after tripping at a subsequent lower threshold until the battery can be recharged/replaced
  - Software overhead is zero once the ACMP is configured and until an interrupt is requested

- **Use the LDMA to move data in EM2 instead of waking the CPU via interrupt**
  - Low frequency IADC scan of analog inputs is a prime example
  - At 1 Hz, current draw is around 100 µA to save the results of an 8-channel scan via interrupt
  - Moving the operation to the LDMA reduces this to around 18.5 µA, a reduction of 5.5x
  - The CPU must wake every 8 samples; the LDMA can save 2048 results before waking the system

Other Techniques

Other possible optimizations

- **Turn off parts of the RAM while staying in EM2 / EM3**
  - FG23 has 64 kB of RAM, consisting of 4 RAM banks of 16 kB each
  - If not needed you can turn off one or more RAM banks in EM2 / EM3
  - Current optimizations is approx. 100 nA per RAM bank
  - However, at least one RAM bank (bank 0) must remain enabled

- **Enable Voltage Scaling in EM2 / EM3 and use VSCALE0 level**
  - The internal voltages will go down to 0.9 V which will reduce the current consumption in EM2 / EM3
  - However, when using voltage scaling, the wake-up time from EM2 / EM3 will slightly increase as the internal regulator will need more time to settle on the higher voltage level that is being used in EM0 / EM1 active mode.

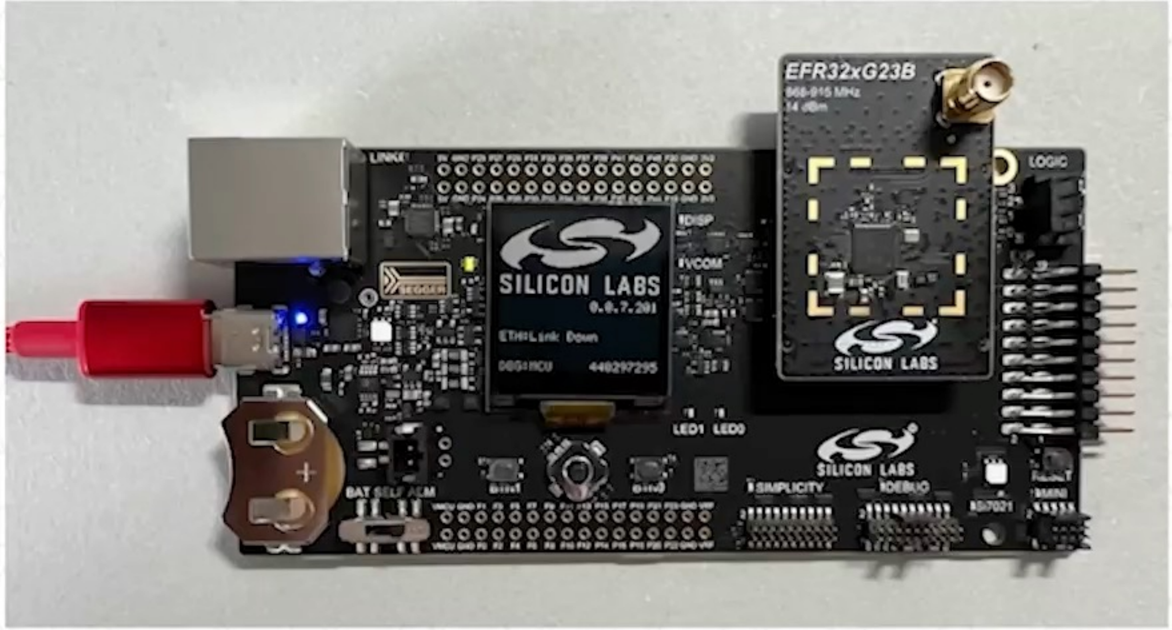
- **Turn off debug interface in EM2 / EM3**
  - If debugging is not needed make sure to not keep the debug interface enabled in EM2 / EM3
  - → Clear the EM2DBGEN bit in the EMU_CTRL register

Other possible optimizations

- **Use LESENSE (on xG23 devices) to automate sensor sampling**
  - LESENSE can automatically sample resistive, inductive and capacitive sensors and will trigger an interrupt once certain sensor conditions are met

- **Reduce active currents (EM0 / EM1) by:**
  - Reducing the clock speed if the application can run at lower speed.
  - E.g. let the application run from HFRCO and reduce its clock frequency to down to 1 MHz

Demo


EFR32xG23B
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Q&A

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