



EFR32FG13 Dual Band Radio Board

2.4 GHz / 915 MHz 19 dBm, VMCU to PAVDD

| Board Function | Page |
|----------------------------|------|
| Title Page | 1 |
| RF, Antenna & Power | 2 |
| EFR32 Signal Assignments | 3 |
| WSTK Connectors & Board ID | 4 |

| Revision History | |
|------------------|-------------------|
| Rev. | Description |
| A00 | Initial revision. |
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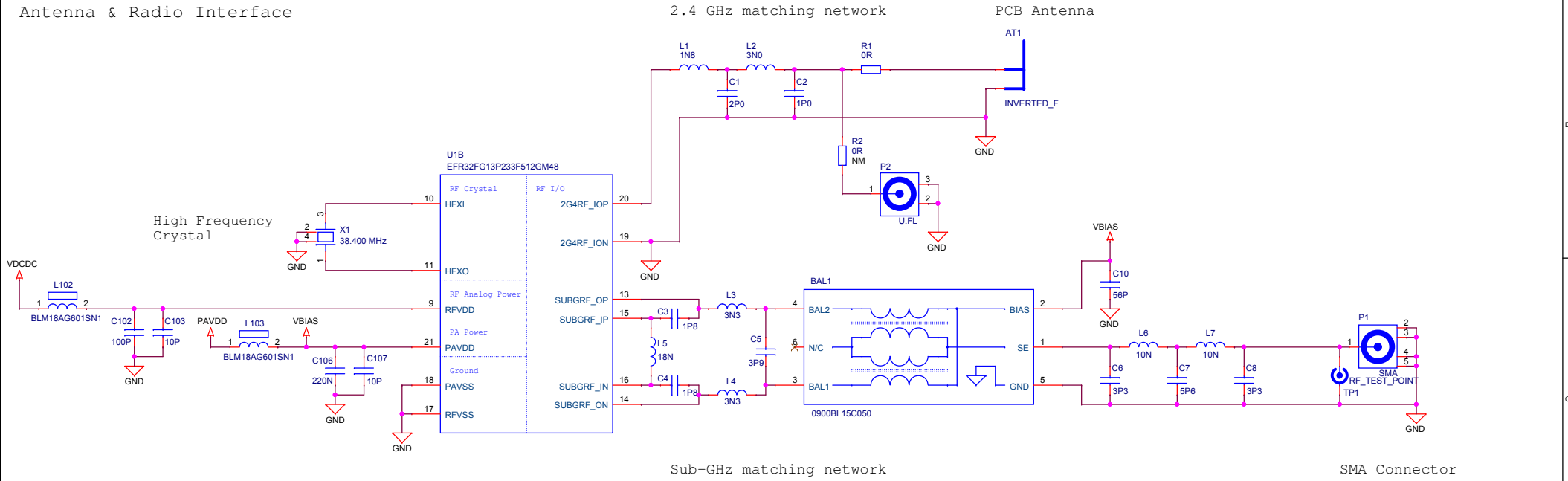
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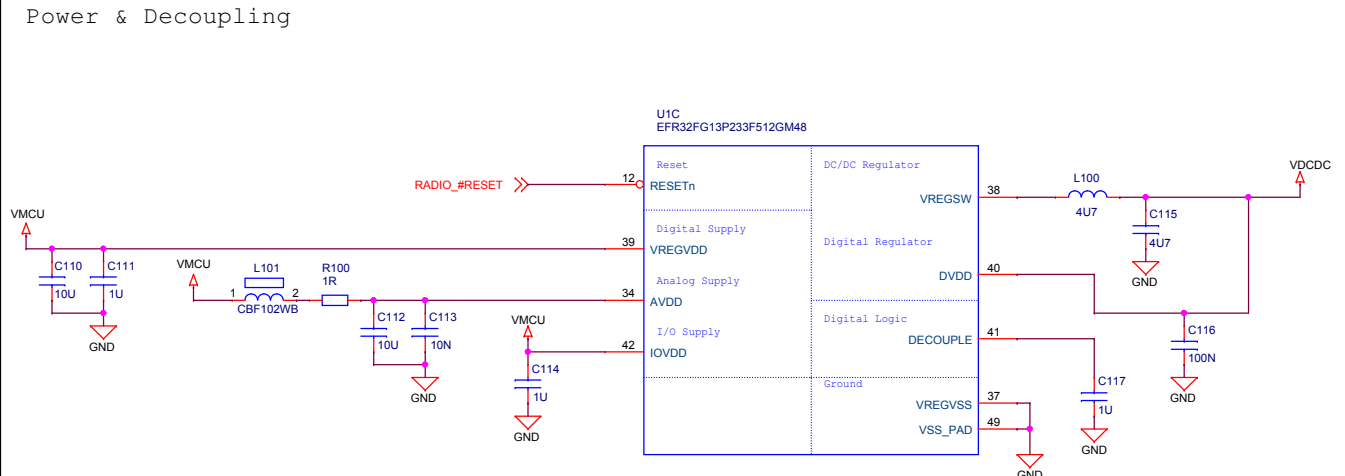
<Schematic Path>
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| | | Schematic Title | |
| | | EFR32FG13 Dual Band 2400/915 MHz Radio Bo | |
| Designed: JSH Approved: JNO | | Page Title | |
| | | Title Page | |
| Size A3 | BOM Doc No: <Cage Code> | Document number | Revision |
| Design Created Date: Monday, April 02, 2012 | | BRD4255A | A00 |
| | Sheet Created Date Monday, April 02, 2012 | Sheet Modified Date Wednesday, March 01, 2017 | Sheet 1 of 4 |

Antenna & Radio Interface

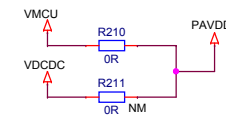


Power & Decoupling

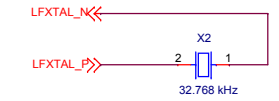


PAVDD Configuration

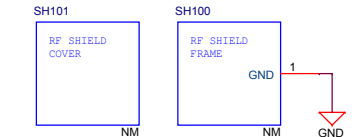
| | Power Config 1 VMCU to PAVDD | Power Config 2 DCDC to PAVDD |
|------|---------------------------------|---------------------------------|
| R210 | Mount | Not mount |
| R211 | Not mount | Mount |



Low Frequency Crystal



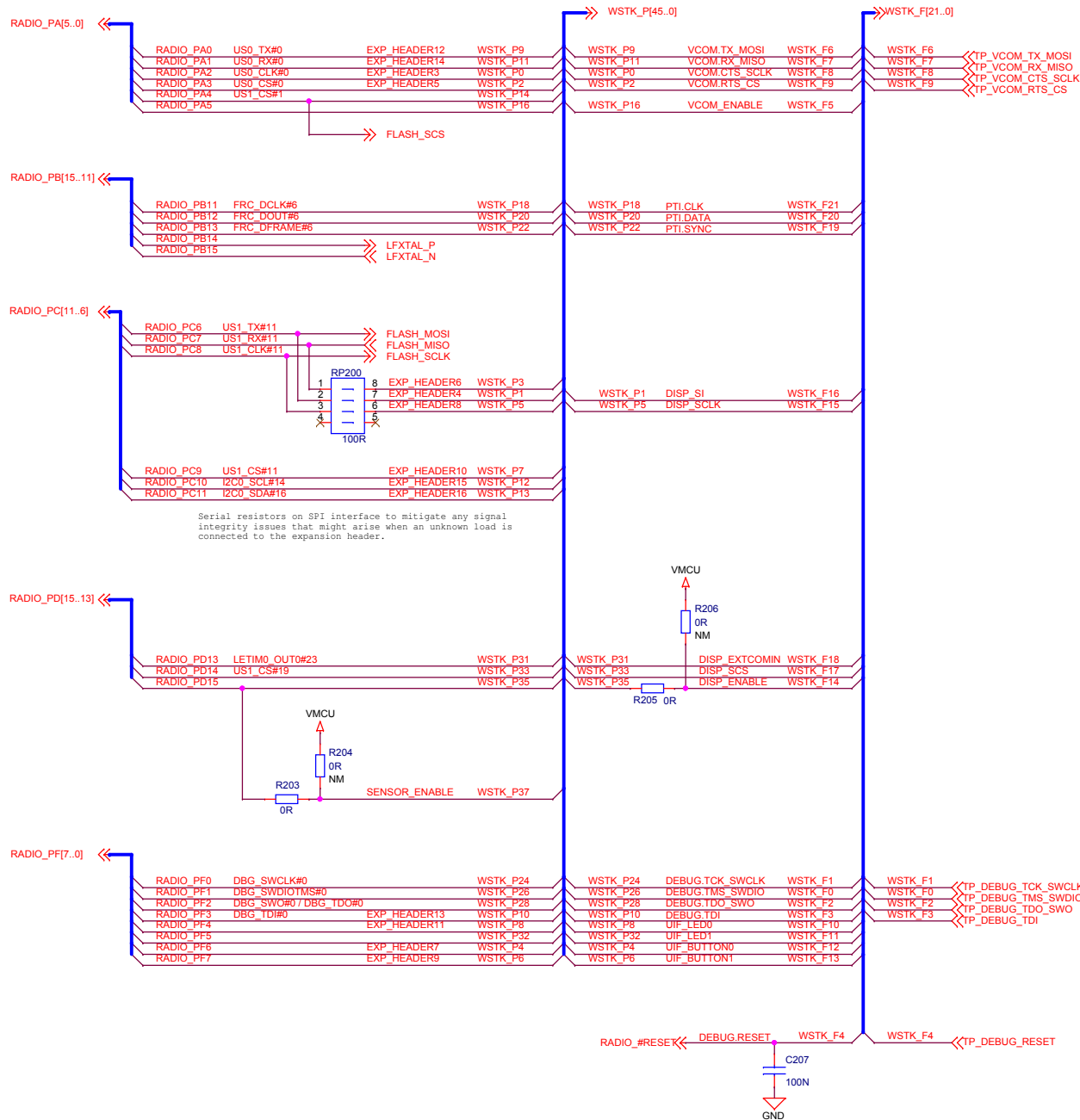
RF Shielding



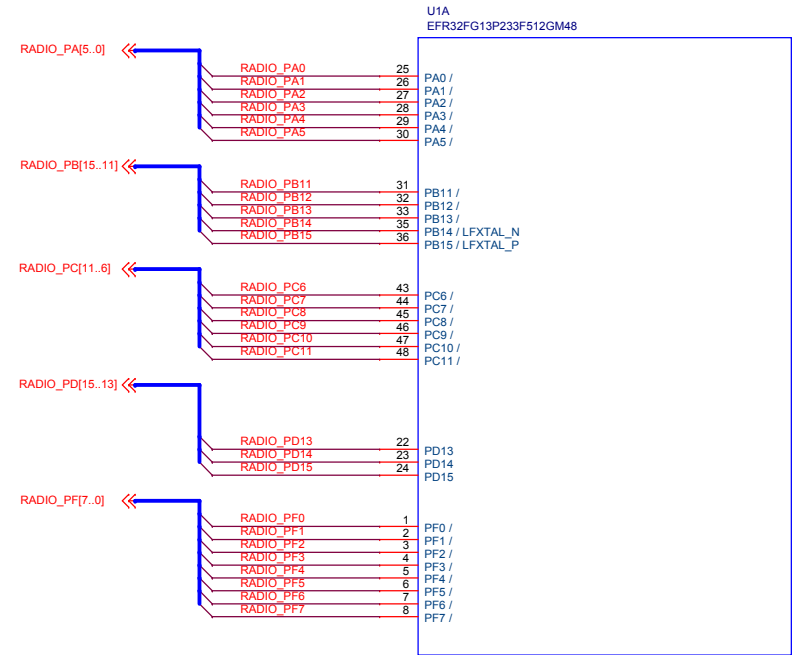
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| | | EFR32FG13 Dual Band 2400/915 MHz Radio Boa | |
| Designed: JSH Approved: JNO | | Page Title | |
| | | RF, Antenna & Power | |
| Size: A3 | BOM Doc No: <Cage Code> | Document number | Revision |
| Design Created Date: Monday, April 02, 2012 | Sheet Created Date: Monday, April 02, 2012 | Document number: BRD4255A | Revision: A00 |
| | Sheet Modified Date: Wednesday, March 01, 2017 | | Sheet 2 of 4 |

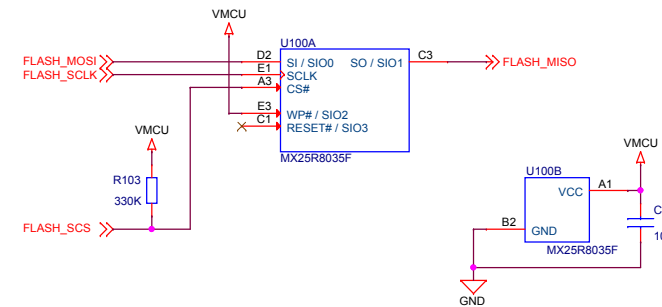
EFR32 Pin Mapping



EFR32 I/O Port Pins



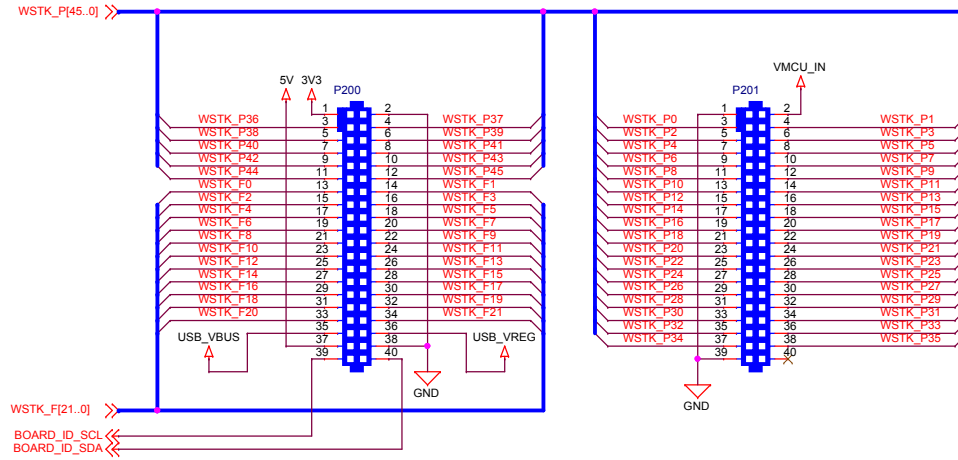
Serial Flash



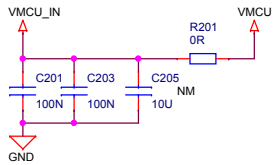
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| | | EFR32FG13 Dual Band 2400/915 MHz Radio Boa | |
| Designed: JSH Approved: JNO | | Page Title | |
| | | EFR32 I/O Port Connections | |
| Size: A3 BOM Doc No: <Cage Code> | | Document number BRD4255A | |
| Design Created Date: Monday, April 02, 2012 | | Sheet Created Date Wednesday, April 11, 2012 | |
| | | Sheet Modified Date Wednesday, March 01, 2017 | |
| | | Revision A00 | |
| | | Sheet 3 of 4 | |

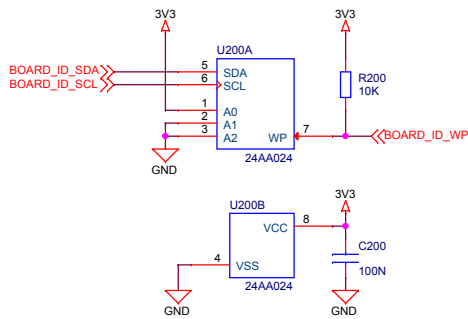
WSTK Connectors



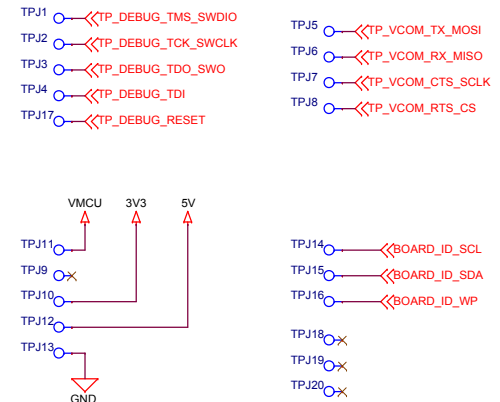
WSTK Power Decoupling




Board Identification



Test Points



<Schematic Path>
SCHEMATIC1

| | | | |
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|  SILICON LABS | | Schematic Title | |
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| Size: A3 | BOM Doc No: <Cage Code> | Document number | Revision |
| Design Created Date: Monday, April 02, 2012 | Sheet Created Date: Tuesday, April 03, 2012 | Document number: BRD4255A | Revision: A00 |
| | Sheet Modified Date: Wednesday, March 01, 2017 | | Sheet 4 of 4 |