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REVISION HISTORY:

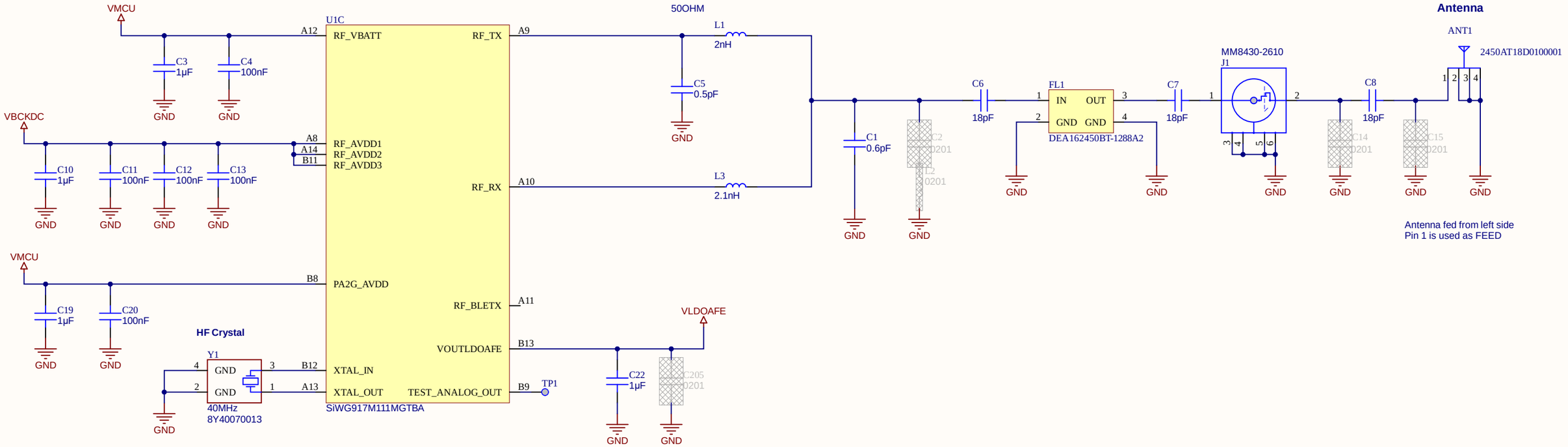
A01	Initial Release
A02	Level shifter (U202) DIR pin connections corrected Load cap values Y2 updated to 12pF

SILICON LABS

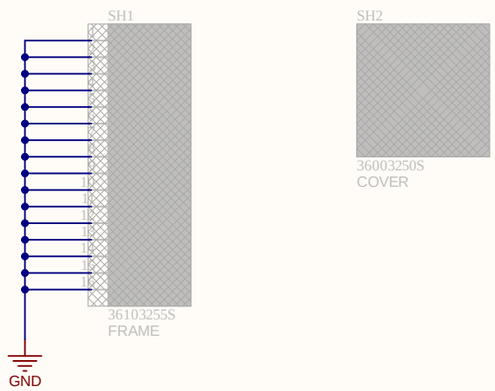
Board name
SiWG917 Wi-Fi and BLE SoC Radio Board
Int.Flash, Ext.PSRAM & Int.RF Switch

Designed	Approved	Page Title	
MSV	RGU	Table of Contents and Revision History	
Size	Sheet Modified Date	Board number	Revision
A3	11/30/2023	BRD4342A	A02 --

SiWG917 RF Frontend (Internal RF Switch + BPF)



EMI Shield



SILICON LABS	Board name: *SiWG917 Wi-Fi and BLE SoC Radio Board Int.Flash, Ext.PSRAM & Int.RF Switch*		
Designed: MSV	Approved: RGU	Page Title: RF Section	
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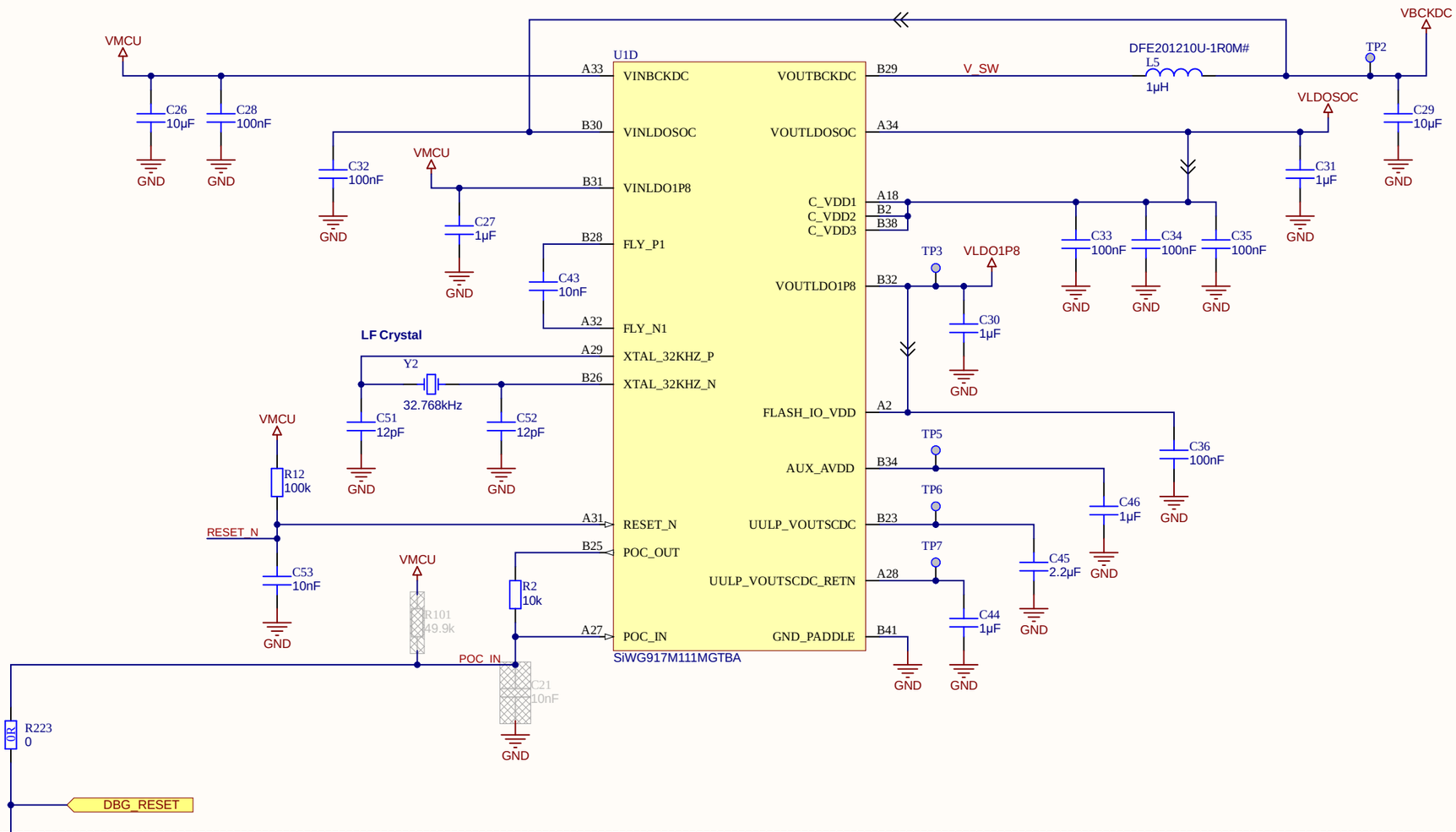
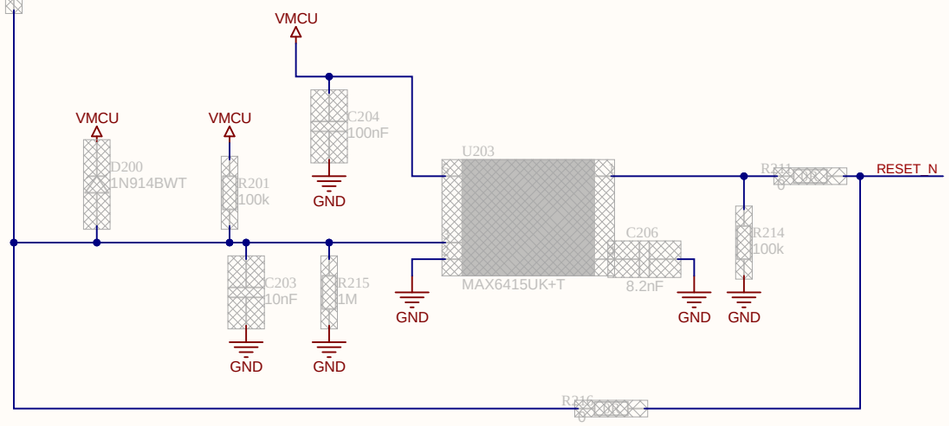
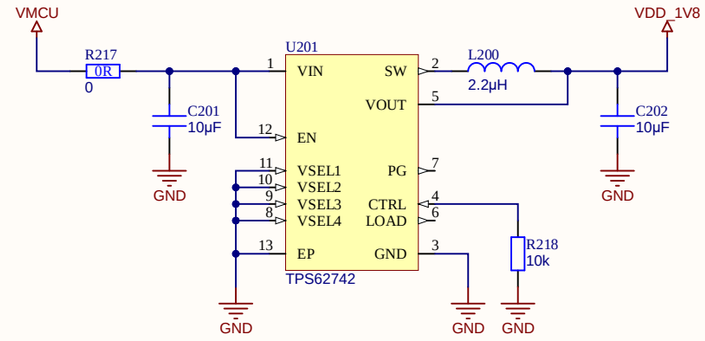
SiWG917 Power



Optional Reset Circuit



DC/DC Regulator for 1.8V Supply



SILICON LABS		Board name: *SiWG917 Wi-Fi and BLE SoC Radio Board Int.Flash, Ext.PSRAM & Int.RF Switch*	
Designed: MSV	Approved: RGU	Page Title: Power Section	
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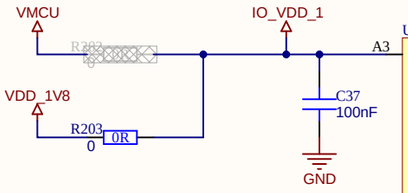
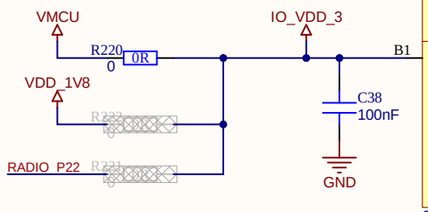
SiWG917 Pin Assignment

IO_VDD_1 Configuration



IO_VDD_3 Configuration



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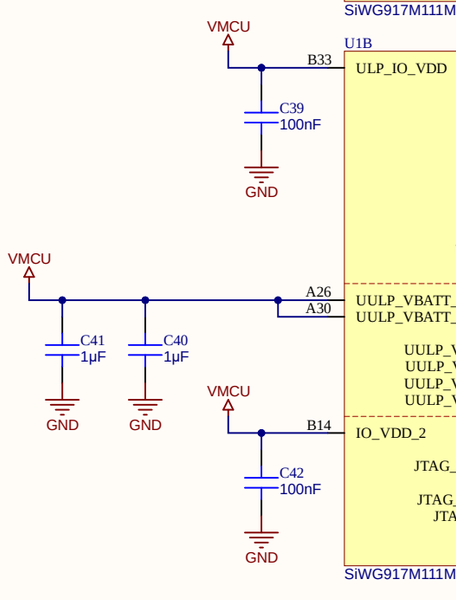
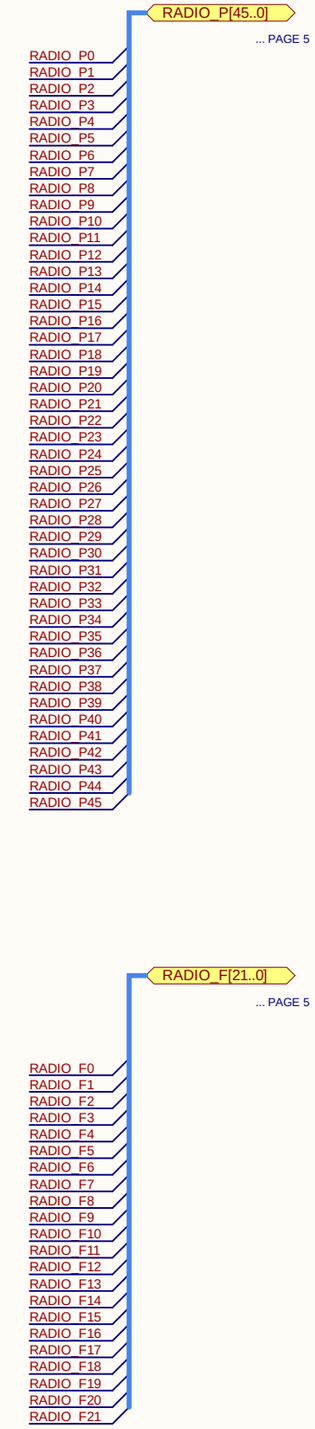
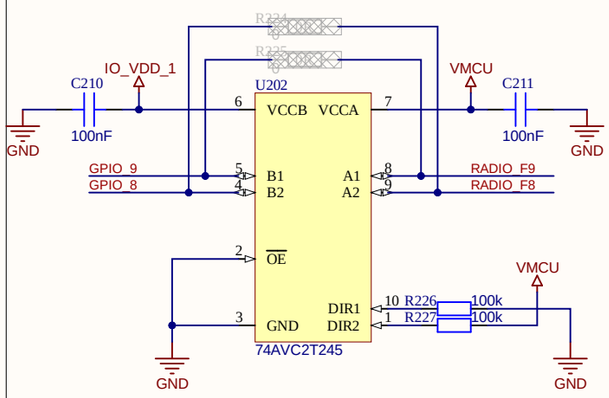


Mainboard Peripheral

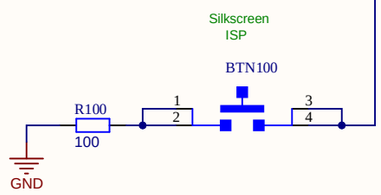
		SiWG917 Peripheral	Connection	Breakout Header Connection	EXP Header Connection	
B20	GPIO_6	GPIO		RADIO_P19		
B19	GPIO_7	GPIO		RADIO_P20		
A20	GPIO_8	TASS_UART1_RX	VCOM_RX	RADIO_F8		
A21	GPIO_9	TASS_UART1_TX	VCOM TX	RADIO_F9		
B3	GPIO_10	GPIO		RADIO_P40		
B4	GPIO_11	GPIO		RADIO_P41		
A4	GPIO_12	MCU_CLK_OUT		RADIO_P21		
A5	GPIO_46	GPIO		RADIO_P24		
A7	GPIO_47	GPIO		RADIO_P26		
B7	GPIO_48	GPIO		RADIO_P28		
B6	GPIO_49	GPIO		RADIO_P30		
A6	GPIO_50	GPIO		RADIO_P32		
B5	GPIO_51	GPIO		RADIO_P34		
A38	GPIO_52	QSPI_PSRAM_SCLK				
B35	GPIO_53	QSPI_PSRAM_SIO0				
A39	GPIO_54	QSPI_PSRAM_SIO1				
B36	GPIO_55	QSPI_PSRAM_CS				
A40	GPIO_56	QSPI_PSRAM_SIO2				
B37	GPIO_57	QSPI_PSRAM_SIO3				
A41	GPIO_15	M4SS_TRACE_CLKIN		RADIO_P23		
B40	GPIO_25	CLK		RADIO_P25		
A1	GPIO_26	CMD		RADIO_P27		
B39	GPIO_27	D0		RADIO_P29		
A44	GPIO_28	D1		RADIO_P31		
A43	GPIO_29	D2		RADIO_P33		
A42	GPIO_30	D3		RADIO_P35		
			JOYSTICK	RADIO_P36		
B22	ULP_GPIO_0	ULP_SPI_DOUT	DISP_SI	RADIO_P16		RADIO_F16
A35	ULP_GPIO_1	GPIO		RADIO_P1		
A37	ULP_GPIO_2	GPIO	UIF_LED0	RADIO_P10		
B21	ULP_GPIO_4	GPIO		RADIO_P3		
A19	ULP_GPIO_5	GPIO		RADIO_P5		
A22	ULP_GPIO_6	ULP_I2C_SDA	SENSOR_SDA		EXP HEADER16	RADIO_P13
B18	ULP_GPIO_7	ULP_I2C_SCL	SENSOR_SCL		EXP HEADER15	RADIO_P12
A36	ULP_GPIO_8	ULP_SPI_CLK	DISP_SCLK	RADIO_P15		RADIO_F15
A24	ULP_GPIO_9	ULP_UART_RX	VCOM RX	RADIO_F7		
A23	ULP_GPIO_10	ULP_SPI_CS0	DISP_SCS	RADIO_P17		RADIO_F17
B17	ULP_GPIO_11	ULP_UART_TX	VCOM TX	RADIO_F6		
B10	UULP_VBAT_GPIO_0	GPIO	DISP_ENABLE	RADIO_P14		RADIO_F14
B27	UULP_VBAT_GPIO_1	GPIO	SENSOR_ENABLE	RADIO_P37		
B24	UULP_VBAT_GPIO_2	WAKEUP	UIF_BUTTON0	RADIO_F12		
A25	UULP_VBAT_GPIO_3	WAKEUP	DISP_EXTCOMIN	RADIO_P18		RADIO_F18
A17	JTAG_TCK_SWCLK	JTAG_TCK/SWCLK	DBG TCK/SWCLK	RADIO_F1		
B16	JTAG_TDI	JTAG_TDI	DBG TDI	RADIO_F3		
A16	JTAG_TMS_SWDIO	JTAG_TMS/SWDIO	DBG TMS/SWDIO	RADIO_F0		
B15	JTAG_TDO_SWO	JTAG_TDO/SWO/ISP_ENABLE	DBG TDO/SWO	RADIO_F2		



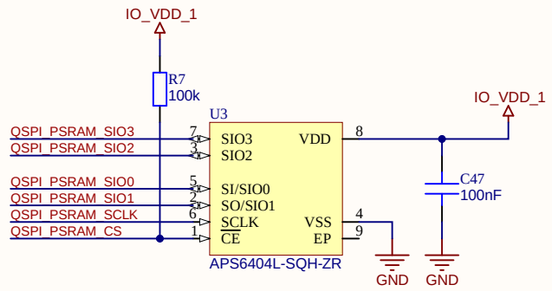
Level Shifter



ISP Mode Button



QSPI PSRAM



SILICON LABS

Board name			
SiWG917 Wi-Fi and BLE SoC Radio Board Int.Flash, Ext.PSRAM & Int.RF Switch			
Designed: MSV	Approved: RGU	Page Title: Pin Assignment and QSPI PSRAM	
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Radio Board Socket

Upper connector

RADIO_P[45..0]
... PAGE 4

RADIO_F[21..0]
... PAGE 4

DBG_RESET
RADIO_F4
... PAGE 3

5V_IN
3V3
Silkscreen

P200

	1	2	
	1	2	
RADIO_P36	3	4	RADIO_P37
	5	6	
RADIO_P40	7	8	RADIO_P41
	9	10	
	11	12	
RADIO_F0	13	14	RADIO_F1
RADIO_F2	15	16	RADIO_F3
RADIO_F4	17	18	
RADIO_F6	19	20	RADIO_F7
RADIO_F8	21	22	RADIO_F9
RADIO_F10	23	24	
RADIO_F12	25	26	
RADIO_F14	27	28	RADIO_F15
RADIO_F16	29	30	RADIO_F17
RADIO_F18	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	39	40	

GND

Lower connector

Silkscreen
VMCU_IN

P201

	1	2	
	1	2	
	3	4	RADIO_P1
	5	6	RADIO_P3
	7	8	RADIO_P5
	9	10	
	11	12	
	13	14	
RADIO_P12	15	16	RADIO_P13
RADIO_P14	17	18	RADIO_P15
RADIO_P16	19	20	RADIO_P17
RADIO_P18	21	22	RADIO_P19
RADIO_P20	23	24	RADIO_P21
RADIO_P22	25	26	RADIO_P23
RADIO_P24	27	28	RADIO_P25
RADIO_P26	29	30	RADIO_P27
RADIO_P28	31	32	RADIO_P29
RADIO_P30	33	34	RADIO_P31
RADIO_P32	35	36	RADIO_P33
RADIO_P34	37	38	RADIO_P35
	39	40	
	39	40	

GND

Mainboard Power Decoupling

VMCU_IN
R219 0R 0
C207 100nF
C208 100nF
C209 10µF
VMCU
GND GND GND

Board ID

3V3 R200 10k
3V3 C200 100nF
3V3
GND GND

U200 M24C02

	8	VCC	E0 1
	7	WC	E1 2
	6	SCL	E2 3
	5	SDA	VSS 4
			EP 9

GND

I2C
SDA
SCL
WP

BOARD_ID_SDA
BOARD_ID_SCL

I2C
WP
SCL
SDA

BOARD_ID_WP
BOARD_ID_SCL
BOARD_ID_SDA

Production Test Points

I2C
SCL
SDA
WP

RADIO_F0	TPJ1	SWDIO
RADIO_F1	TPJ2	SWCLK
RADIO_F2	TPJ3	SWO
RADIO_F3	TPJ4	TDI
RADIO_F4	TPJ17	RESET
RADIO_F6	TPJ5	VCOM TX
RADIO_F7	TPJ6	VCOM RX
RADIO_F8	TPJ7	VCOM CTS
RADIO_F9	TPJ8	VCOM RTS
BOARD_ID_SCL	TPJ14	BOARD ID SCL
BOARD_ID_SDA	TPJ15	BOARD ID SDA
BOARD_ID_WP	TPJ16	BOARD ID WP
	TPJ18	USB DP
	TPJ19	USB DM

VLDOSOC 3V3 VMCU 5V_IN

VRF	TPJ9
3V3	TPJ10
VMCU	TPJ11
5V	TPJ12
GND	TPJ13

GND

LOGO1
SILICON LABS
LOGO SILABS 14MM

MARK1 RoHS
MARK2 ESD
MARK3 Pb-free
MARK4 BOARD INFO FRAME

SILICON LABS

Board name
SiWG917 Wi-Fi and BLE SoC Radio Board
Int.Flash, Ext.PSRAM & Int.RF Switch

Designed	Approved	Page Title
MSV	RGU	Radio Connectors and Board ID

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